Thermal Mitigation Strategy for Backside Power Delivery Network

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***Abstract*—By improving power delivery capability and mitigating signal routing congestion, Back Side Power Delivery Network (BSPDN) has been proven to be a game changer for the next generation of chip design. However, it also brings thermal challenges due to a significantly larger thermal resistance between the CPU power grid and on-chip forced cooling. Therefore, a cutting-edge cooling scheme is needed to tackle this issue. Inspired by the similarity between Back End of Line (BEOL) layer structure and 3D manifolded microchannel cooler, we propose an innovative embedded microchannel cooling configuration to bring the coolant closer to FEOL, which also cooperates with chip-top jet cooling to form a dual-sided cooling system. Finite Element Analysis (FEA) is performed to study the thermal performance of chips and cooling effectiveness and efficiency for microchannel cooling. Due to the high complexity of a detailed BSPDN model, several engineering approaches are utilized to reduce the computing resource requirement. Detailed Back End of Line (BEOL) thermal models are established and investigated for computing its accurate orthotropic thermal conductivity. Then, a local unit cell model including both BSPDN chip and coolant region are simulated through system coupling approach, after which the effective Heat Transfer Coefficients (HTC) are extracted and applied to a 50 µm × 50 µm overall model with power map heat source. A control parameter study is conducted by varying coolant type of water and air, inlet flow velocity, and inlet flow temperature. It turns out that the microchannel cooling with 283K, 0.06m/s water inlet can reduce the maximum temperature by more than 20% or about 20°C for both uniform heat flux and heat map cases, at an expense of 2581 Pa inlet pressure.**

Keywords—BSPDN, Airgap cooling, Embedded microchannel cooling, BEOL.

I. INTRODUCTION

In the semiconductor industry's roadmap, improvements in chip power, performance, and area (PPA), including CPUs and memory components like SRAM and DRAM, have traditionally been driven by the front end of line (FEOL) process. As semiconductor technology approaches its physical limits, the Back End of Line (BEOL), Middle of Line (MOL), and packaging phases have gained importance in shaping and enhancing chip and system PPA. The implementation of 3D integration technology has notably improved 3D system such as SRAM-on-Logic system PPA by optimizing memory-to-logic connections [1]. Additionally, backside interconnect, integrated inside or beneath the silicon substrate, offers a valuable complement to the traditional chip BEOL [2]. Using backside interconnect for backside power delivery etc. has been widely regarded a game changer for improving chip PPA in technology nodes beyond 2nm with both 2D and 3D chip configurations. Furthermore, backside interconnect is also an essential part of the very advanced transistor CFET (Complementary Field Effect Transistor, with normally PMOS stacking on top of NMOS) [3].

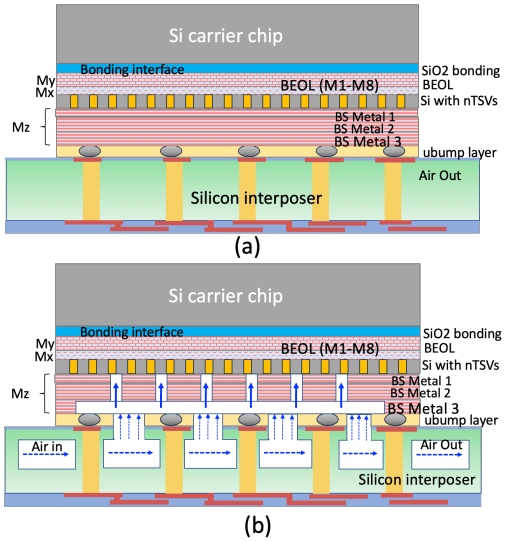

Figure 1: Schematic of the BSPDN package structure: (a) conventional package layer inside the BSPDN architecture; (b) Our proposed concept of embedded microchannel cooling inside the BEOL layer using airgap as the cooling channels.

The Backside Power Delivery Network (BSPDN) enhances the power delivery capabilities and alleviates signal routing congestion on the chip's front side. Moreover, it facilitates the routing of global signals like SRAM macro addresses, data signals, and other lengthy logic signals (e.g., clock tree) beneath the substrate, enhancing integrated circuit (IC) performance and power efficiency. In our previous research [3], we numerically compared the thermal performance of a 300 nm substrate BSPDN in Fig.1(a) with the conventional 300 µm Si substrate frontside power delivery network (FSPDN) in Fig.1(b). The results showed that BSPDN exhibited higher temperatures and approximately a 45% increase in CPU hotspot area. Detailed analysis revealed that BSPDN's higher thermal resistance (from the FEOL to the cooler, assumed in the carrier wafer side) result from the existence of BEOL layer, silicon oxide bonding interface as well as the thinned silicon layer, causing reduced vertical and lateral heat spreading respectively and hence more

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significant temperature hotspots [4-7]. The BEOL stack and bonding oxide increase thermal resistance toward top and impedes the effective removal of heat generated at the active transistors. Another significant concern with implementing BSPDN is the potential issue of self-heating due to the extreme substrate thinning.

Previous studies [3,5] indicate that thermal resistance in BSPDN is primarily influenced by its BEOL and bonding interface required for the carrier. Thinning the substrate results in increased horizontal thermal resistance and consequently decreased lateral heat spreading, leading to more temperature nonuniformity due to hot spots compared to FSPDN and also higher maximum temperature in a chip. Reference [5] highlighted the need to explore innovative cooling approaches for BSPDN designs to effectively tackle the challenge of self-heating, similar to the thermal challenges in 3D stacked chips. Reference [6] researched the impact of different metals and ratios of substrate and backside dielectric thickness on temperature, providing design guidance for BSPDN. Reference [7] investigated the thermal impact of Si substrate thickness, backside metals, and μTSV density to evaluate the balance between the advantageous and adverse thermal effects of the BSPDN. Wei et al., proposed a dual-sided cooling utilizing topside microjet cooling and glass/silicon interposer embedded microchannel cooling is proposed to address the thermal bottleneck of BSPDN configurations owing to the lower thermal conductivity SiO_2 bonding layer [8].

II. Novel Concept: Embedded Airgap Cooling in BEOL Layer

In response to these challenges, our group systematically explores methods for mitigating thermal issues within the BSPDN package structure using numerical modeling approach. Solutions include conduction heat spreading and advanced convection cooling techniques [8]. Convection cooling solutions encompass laminate substrate cooling customization as well as top-side microjet cooling [9-11]. Conduction solutions involve enhancing the thermal conductivity of the silicon wafer carrier bonding layer and introducing diamond-filled underfill between the die and laminate substrate, along with an embedded diamond heat spreader.

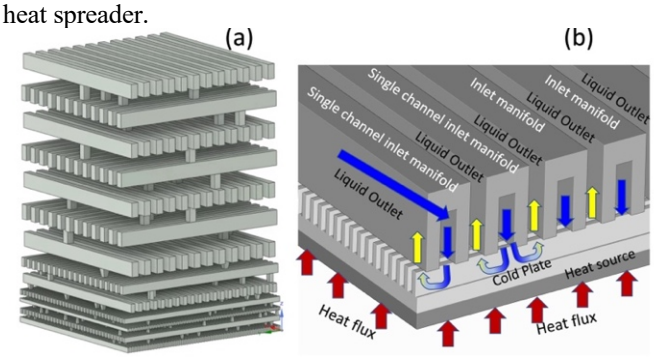


Figure 2: Similarity between (a) BEOL layer structure (b) the multi-level 3D manifolded microchannel cooler.

In the thermal science community, manifold based embedded multi-layer microchannel cooling shows great potential over conventional cooling method. The Embedded Microchannels-3D Manifold μ-Cooler (EMMC) shown in Fig.2(b) present a promising solution to reduce the pressure drop and enhance overall thermal performance [12-16]. This design facilitates the vertical routing of fluid by delivering cold liquid from the top and collecting hot fluid through adjacent outlet channels. Notably, fluid elements only traverse a short distance (L1) in the cold plate (CP) channel with a small hydraulic diameter, in contrast to the much longer distance (L) in traditional coolers. For the typical BEOL structure shown in Fig.2(a), the different BEOL layers are designed with different metal layers are perpendicular with each other. This structure shows similar geometry features as the 3D EMMC structure, which provide a novel cooling strategy using BEOL and airgap structure.

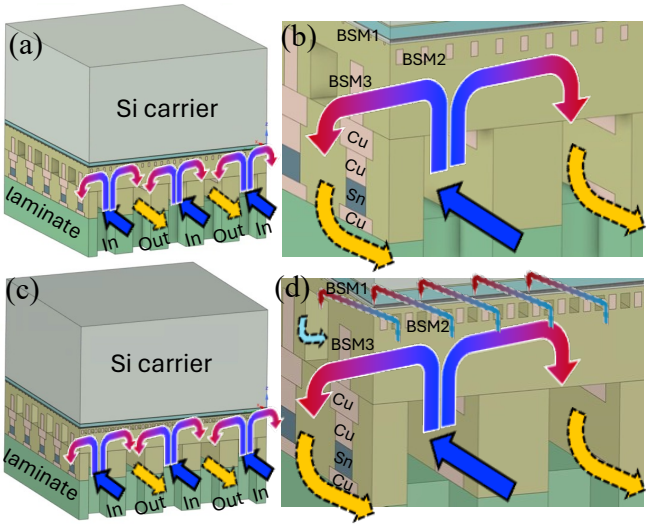


Figure 3: Proposed embedded microchannel cooling inside the backside BEOL layer: (a-b) BSPDN with 2-layer-microchannel cooling: microchannel etched through micro bump layer and Back-Side Metal 3 (BSM3) layer; (c-d) BSPDN with 3-layer-microchannel cooling etched through to BSM2 layer.

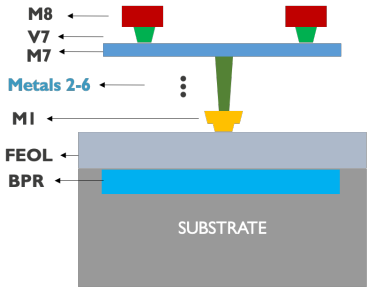
In this work, an air-gap microchannel cooling scheme is proposed, which has two different designs, as shown in Fig.3. One with microchannel etched through micro bump layer and Back-Side Metal 3 (BSM3) layer, as illustrated in Fig.3(a-b). The other one more aggressively extends microchannel to BSM2 layer, shown in Fig.3(c-d). The coolant flow is firstly led from bottom to impinge on the lower surface of BSM3 layer, then redirected along the microchannel in micro bump region (main channel). The pressure gap between inlet side and outlet side and the momentum of flow will push the coolant to fill in microchannels in BSM3 layer and BSM2 layer (sub-channels). The flow direction will then be reversed after flowing out from sub-channels and get drained out from the microchannel system. Although the 3-layer-microchannel scheme shown in Fig.3(c-d) is considered more effective at heat removal rate since it brings coolant even closer to heat source, it can lead to additional challenges to mechanical reliability. Therefore, in this work, only the 2-layer-microchannel scheme shown in Fig.3(a-b) is investigated.

The combined implementation of these solutions is expected to yield an improvement in BSPDN thermal performance compared to the conventional thermal cooling approach, bringing it closer to the performance of the frontside counterpart. This research aims to provide a comprehensive set of thermal design guidelines for the BSPDN architecture, thereby advancing chip PPA in advanced technology nodes.

III. MOLDEING METHODOLOGY: MULTI-SCLAE MODELING

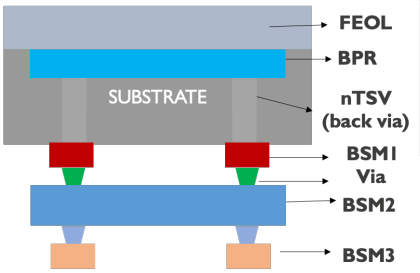
A. Modeling geometery and parameters

The BSPDN chip modeling consists of three main regions: 1) front side region, 2) back side region 3) cooling fluid domain. The front side region from bottom to top includes BEOL, FEOL, SiO_2 bonding, and silicon carrier. The bonding and FEOL have a thickness of 100 nm and 50 nm, and their thermal conductivities are set isotropic as 1.2 W/(m·K) and 1.5 W/(m·K) . A 9-layers BEOL geometry at A14 node (Mint-M8) is used in the thermal modelling. Because of Cu diffusion effect, Ru is applied to small scale metal lines Mint-M3 and vias V0-V2, which are very close to FEOL. The rest of metal lines and vias are all Cu. The thermal conductivity of 0.3 W/(m·K) is used for low-k dielectric material layer. The detailed geometry parameters for metal lines and vias can be found in Fig.4.



Metal layers (directions)	Width/height/pitch
Mint	9 nm/27.5 nm/18 nm
M1	14 nm/28 nm/28 nm
M2	9 nm/18 nm/18 nm
M3	14 nm/28 nm/28 nm
M4 /M5	24 nm/48 nm/48nm
M6~M8	40 nm/80 nm/80 nm
V0	24 nm
V1	31.5 nm
V2	24 nm
V3	30 nm
V4/V5	48 nm
V6/V7	80 nm

Figure 4: BEOL with M0-M8 modeling configuration and metal layer parameters for BSPDN at A14 node.



Metal layers (directions)	Width/height/pitch
BPR	30 nm/0.18um/90nm
BSM1	0.2um/0.2um/2.1um
BSM2	0.5um/1um/1.8um
BSM3	2um/4um/10um
nTSVs	90nm to 120nm

Metal vias	height
nTSVs	120nm
BSM1-BSM2	0.2um
BSM2-BSM3	1um

Figure 5: Backside parts modeling configurations and metal layer parameters for BSPDN at A14 node.

The back side region of the BSPDN chip incorporates BPR, nTSVs, thinned Si substrate, BSM1-3, two layers of BS vias (connecting BSM1-BSM2 and BSM2-BSM3), BS dielectric, micro bumps, and underfill of bump layer. The model at thinned Si substrate part is simplified to reduce the computing difficulty. The 180 nm thick BPR and 120 nm height nTSVs are exactly embedded into the thinned Si substrate with a thickness of 300 nm. The nTSV has a shape of frustum with small end side length equal to 90 nm that connects to BPR, and 120 nm large end connecting to BSM1. The metal interconnect material for BPR and nTSVs are both set to be tungsten (W).

Fig. 5 illustrates specific geometric parameters for all BSMs and vias, each designated as copper (Cu). The micro bump comprises Cu pads with 25 µm in length, with one layer at the top die having a thickness of 2 µm and the other at the bottom die with half the thickness. A cylindrical Cu bump and Sn bump are interconnected in the center, both having a thickness of 2 µm and a diameter of 3 µm. To have an accurate thermal modelling based on Fourier's law, dimension-dependent thermal conductivities extracted from Monte Carlo Boltzmann transport equation (BTE) are utilized, considering scattering effect for nanoscale interconnections [17]. Fig. 6 illustrates modeling and meshing challenges, emphasizing the complexity in establishing a highly detailed model for BSPDN due to the large-scale feature size differences ranging from 20 nm to 25 µm. Therefore, various thermal modeling techniques are employed to address these challenges, such as effective layers and unit cell modeling [17].

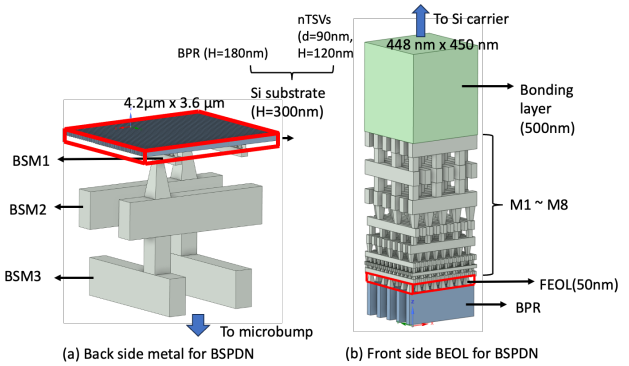


Figure 6: Geometry complexity challenge: (a) Detailed back-side metal will be built into the overall model; (b) Effective thermal conductivity of front side BEOL should be extracted for the complexity of detailed modeling.

B. Equivalent BEOL model

The significance of thermal conductivity of the BEOL has becoming more and more crucial within 3D stacking systems, particularly with the reduction of chip thickness into the submicron range. The thermal resistance of the BEOL layer has emerged as a dominant factor influencing the overall thermal dissipation in 3D integration systems. Therefore, it is necessary to precisely extract the effective thermal conductivity in both out-of-plane and in-plane directions.

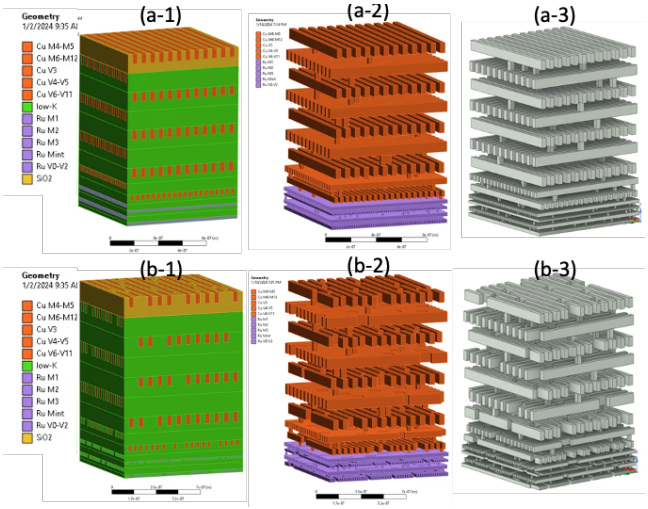


Figure 7: Detailed model for BEOL: (a) 1% via density and 50%-line density barrierless; (b) 1% via density and 45%-line density barrierless.

A 1µm×1µm unit cell from an advanced 13-metal layer BEOL structure, specifically Mint-M12, representative of the 3 nm logic technology node, is simulated and analyzed using the

finite element method. In Fig. 7, two BEOL geometries are illustrated: one with a 1% via density and 50% line density, and the other with a 1% via density and 45% line density, both being barrierless metal structures. To extract the equivalent out-of-plane thermal conductivity of the BEOL, a uniform external heat flux q is applied at the bottom end, and the average heat flux through any internal surface is calculated using Equation (1). Due to the 1D-type heat conduction model, the surface average heat flux exhibits minimal variation along the vertical direction. The average temperature for the top and bottom surfaces is employed to calculate the temperature difference across the entire BEOL in the vertical direction, and this methodology is referred to as the "all-in-one thermal conductivity extraction" in this paper. Utilizing the simplified Fourier's law presented in Equation (2), the equivalent out-of-plane thermal conductivity is computed. The boundary condition employed for this extraction in the work is depicted in Fig. 8.

$$\bar{q} = \frac{\iint q dA}{A} \tag{1}$$

$$k_{eq} = \frac{\bar{q}L}{T_h - T_c} \tag{2}$$

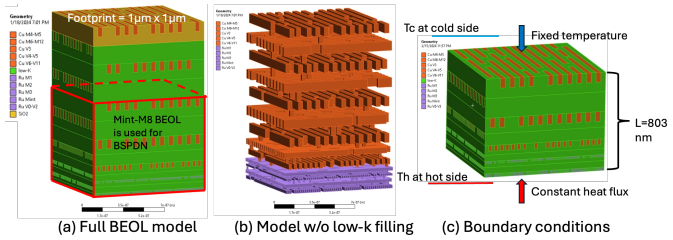


Figure 8: 12-layers BEOL geometry at A14 node. First 9 layers (Mint-M8) are taken for BSPDN BEOL modelling: (a) full BEOL FEM model; (b) FEM model with metal lines only; (c) boundary conditions for BEOL thermal conductivity extraction.

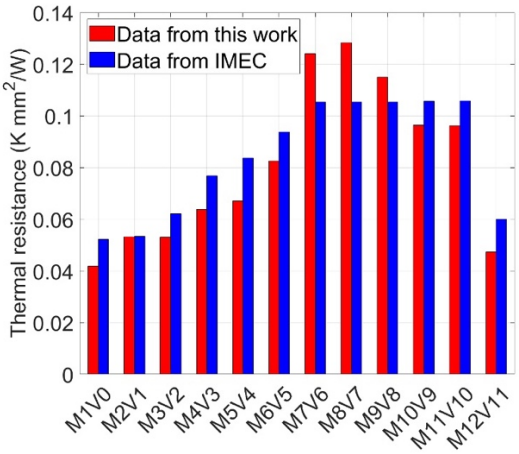


Figure 9: Effective BEOL thermal modelling validation by comparing thermal resistance results from this work with published data from IMEC. M_6V_5-$M_{11}V_{10}$ in IMEC data [17] use low-k 3.0 for dielectric.

The out-of-plane thermal conductivity for the scenario with '1% via density and 45%-line density' is determined to be 1.53 W/(m·K) using the all-in-one BEOL thermal conductivity extraction method. Additionally, a separate validation method is employed, referencing IMEC data from [17], where thermal resistance and thermal conductivity for each MiVi-1 layer are individually examined. The validation results, depicted in Fig. 9, demonstrate a strong agreement. Similarly, the in-plane thermal conductivity is computed for both the 45%-line density BEOL and the 50%-line density BEOL. While the out-of-plane thermal conductivity exhibits only a slight difference due to via density dominance, a significant distinction can be observed for in-plane thermal conductivity. The Mint is oriented along the x-direction, with calculated values of 27.71 W/(m·K) in the x-direction and 21.98 W/(m·K) in the y-direction for the 50%-line density model. In contrast, for the 45%-line density model, the values are 9.77 W/(m·K) in the x-direction and 8.07 W/(m·K) in the y-direction. This discrepancy is attributed to the high line density dependence for in-plane thermal conductivity. In the subsequent study, the effective thermal conductivity for '1% via density and 45%-line density' is utilized.

C. Multi-scale modeling approach

A comprehensive unit cell model incorporating an effective BEOL layer is constructed for finite element modeling and analysis of the BSPDN chip's thermal performance. This includes investigating the thermal relationship between the solid and fluid domains, as well as examining the detailed fluid pressure and velocity fields. The fluid domain is discretized with a total mesh count of 331,086 elements, while the solid domain of the BSPDN chip comprises 2,029,999 mesh elements. The geometric and mesh details for both the solid and fluid domains of the unit cell model are illustrated in Fig.10 and Fig.11, respectively.

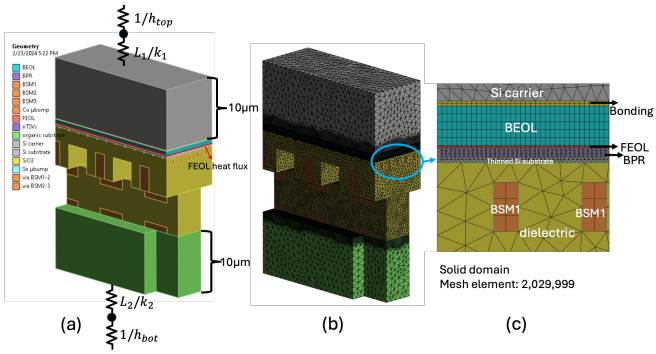


Figure 10: Unit cell BSPDN chip model: (a) unit cell chip geometry and simplified partial 1D thermal network; (b) and (c) mesh details for unit cell chip modelling.

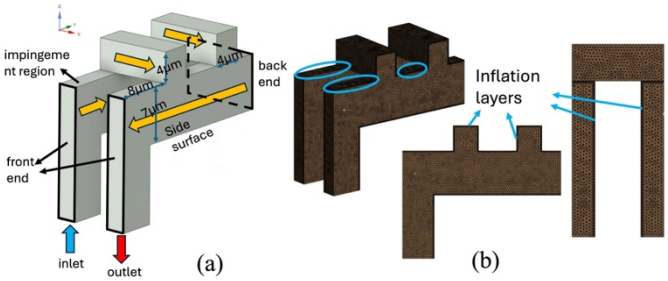


Figure 11: CFD domain for unit cell BSPDN chip: (a) unit cell model fluid domain geometry; (b) mesh details for unit cell fluid domain modelling.

In the thermal modeling of the solid domain, a brief mesh sensitivity study is undertaken to verify that the number of mesh elements is sufficient for obtaining accurate results. Regarding Computational Fluid Dynamics (CFD), Reynolds number (Re)

is computed for all cases, and its values are considerably lower than those associated with turbulent flow. Consequently, the laminar model with the energy equation is adopted for all fluid simulations. The solution method is configured as SIMPLEC (Semi-Implicit Method for Pressure Linked Equations-Consistent), utilizing a least squares cell-based approach for gradient discretization. Pressure, momentum, and energy are all set in a 2nd order format. For each case, the mass flow and velocity at the inlet and outlet surfaces are monitored to ensure both mass conservation and momentum conservation. The Ansys system coupling model for steady-state thermal and Fluent is employed for the unit cell model. Co-convergence for both CFD and thermal modeling is imperative, with convergence criteria set at 1e-4 for temperature and heat flux data transfer across all fluid-solid contacting boundaries. The Si carrier and laminate substrate are only partially modeled due to their significantly larger thickness compared to other components, with original thicknesses of 500 µm and 1.4 mm, respectively. To estimate the equivalent heat transfer coefficient, Equations (3) and (4) are employed for the top surface of the 10 µm Si carrier and the bottom surface of the 10 µm laminate. Given that microchannel cooling alone is insufficient, chip-top jet cooling is implemented to establish a dual-sided cooling scheme. The jet cooling heat transfer coefficient (h_{top}) is defined as 1.96e+4 W/(m²·K), based on nozzle design and Reynolds number-Nusselt number correlations in [8], considering a water jet flow rate of 1 LPM. The bottom cooling heat transfer coefficient (h_{bot}) is set at 20 W/(m² · K), with L1 and L2 representing the original thicknesses subtracting 10 µm. Thermal conductivity values (k1 and k2) are specified as 140 W/(m·K) for the Si carrier and 10 W/(m·K) for the laminate in the vertical direction. Consequently, the effective heat transfer coefficients for the top and bottom surfaces are calculated to be 18,342 W/(m²·K) and 19.94 W/(m²·K), respectively.

$$h_{equ_{top}} = \left(\frac{1}{h_{top}} + \frac{L_1}{k_1}\right)^{-1} \quad (3)$$

$$h_{equ_{bot}} = \left(\frac{1}{h_{bot}} + \frac{L_2}{k_2}\right)^{-1} \quad (4)$$

In the CFD modeling setup, velocity inlet and zero pressure outlet boundary conditions are established. The side surfaces, front ends, and back ends are assigned symmetry boundary conditions. Any other walls act as fluid-solid contacting surfaces, serving as the system coupling region between chip thermal modeling and CFD. To capture detailed fluid behavior near the boundaries, five finely refined boundary layers are meshed. These layers help ensure accurate representation of fluid dynamics and heat transfer characteristics in the vicinity of the boundaries.

To incorporate a power map into the FEOL heat source, a larger finite element model measuring 50 µm by 50 µm is constructed. The boundary conditions and the applied power heatmap within a specific region of the CPU are outlined below. The BEOL layer for BSPDN Mint-M8 is represented with an equivalent orthotropic thermal resistance, while BS-M1-M3 are modeled in detail, as depicted in Fig. 12. The hybrid bonding model is employed to connect the Power Delivery Network (PDN) to the bottom laminate. It's important to note that although Backside Reflectors (BRP), nanoscale Through-Silicon Vias (nTSVs), and the thinned 300 nm silicon substrate are detailed in the figure, their highly patterned geometries necessitate the use of an effective layer for simulation. This approach is adopted due to the considerable computational resources required to handle the numerous solid-solid contacts. Similar to this, an orthotropic effective thermal conductivity study is conducted, revealing values of 55.4 W/(m·K), 58.3 W/(m·K), and 57.6 W/(m·K) in the x, y, and z directions, respectively. The orientation of the Backside Reflector (BPR) is aligned with the y-direction. The total number of mesh elements for the entire model is 1,885,979.

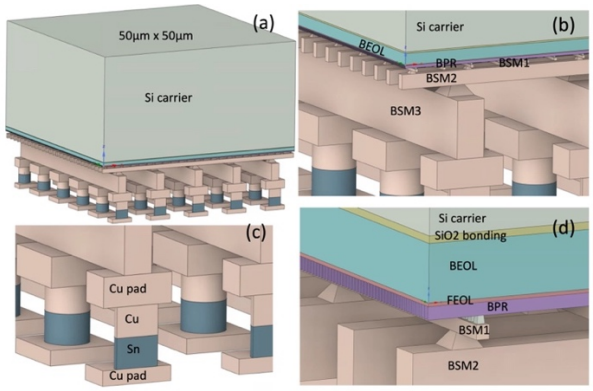


Figure 12: Detailed overall model utilizing effective BEOL for model simplification. Laminate, micro bump underfill and thinned substrate are not displayed: (a) overall 3D view; (b) zoom in for BS layers; (c) zoom in for micro bump geometry without underfill; (d) zoom in for front side geometries.

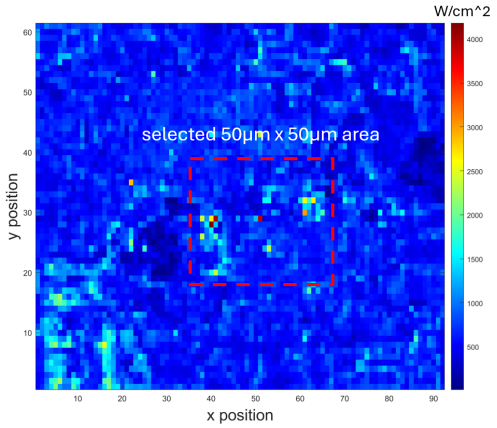


Figure 13: High-performance chip power map, overall average power density = 656 W/cm^2, local average power density for selected region = 711 W/cm^2. Total size 132.768 µm by 132.948 µm. x and y label represents pixel index. Each pixel corresponds to a real size 1440 nm by 2160 nm.

In Fig.13, a high-performance chip power map is presented, and a local region measuring 50 µm by 50 µm is identified due to its high power density deviation [18]. This non-uniform heat source is then applied to the Front-End of Line (FEOL) for thermal analysis. Additionally, a baseline investigation is conducted for the case of a uniform heat flux of 711W/cm². Given the high heat flux involved, the chip-top cooling scheme is modified to accommodate a 3 LPM water inlet, accompanied by a topside jet cooling with copper inverse opals (CIOs) microporous structure enhancement to prevent overheating. The

effective heat transfer coefficient, calculated using Equations (3) and (4), is determined to be 80,104 (W/m²·K).

IV. Results and Discussion

A. Unit cell model CFD analysis

In this section, the fluid conditions in thermal fluid coupling numerical simulations are explored under various inlet coolant types and inlet velocity boundary conditions. Recognizing that the stress tolerance for a chip varies based on several aspects of the production process, the magnitude of the inlet velocity is restricted. Specifically, it is ensured that the maximum flow pressure in the channel remains below 3500 Pa to prevent potential mechanical damage to the BEOL structure.

Fig.14 illustrates the flow velocity vector field and streamlines, utilizing air cooling with a 5 m/s inlet velocity as an example, based on the assumption of laminar flow field similarity for all simulation cases. The inlet flow exhibits the highest velocity, subsequently bifurcating into two sub-microchannels in the BEOL region. Relatively lower velocities are observed in the vicinity of the impingement region and the region between two adjacent sub-microchannels. The lowest velocity magnitude near the most downstream boundary (back end) results from flow collision in opposite directions, following the conservation of momentum. Cross-sections A-A and B-B are defined as the center planes of the 1st and 2nd sub-microchannel in the streamwise direction of the inlet flow, respectively. Intuitively, the sub-microchannel closer to the inlet generally exhibits an overall higher velocity magnitude, ensuring a greater heat removal capability.

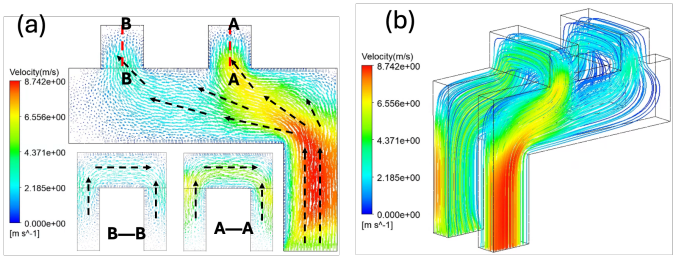


Figure 14: Flow field visualization for air microchannel cooling with inlet velocity=5 m/s: (a) velocity field with cross-sections A-A and B-B; (b) streamline visualization.

To better understand the flow velocity and pressure characteristics, flow velocity and pressure profiles of main microchannel in micro bump region are plotted along the center line, shown in Fig.15(a) and Fig.15(b), respectively. Both water coolant and air coolant are considered with 3 different inlet velocities for each. In the velocity plot, only the inlet side velocity profile is depicted since it closely resembles that of the outlet side. It is observed that the largest velocity magnitude occurs as the inlet flow is about to enter the 1st sub-microchannel. This magnitude experiences a higher percentage increase with increasing inlet velocity. For instance, there is a 25% velocity increase for air flow with a 2 m/s inlet, while it rises to 36% for air flow with a 5 m/s inlet.

In Fig.15(b), the pressure plot is presented for the same inlet coolant types and inlet velocity conditions as the velocity plot, with both inlet side and outlet side tracking lines considered. The pressure magnitude shows an overall continuous reduction along the fluid flowing direction and a relative stability is achieved near the back end of the main microchannel. This pressure stable region approximately overlaps with the low velocity region presented in Fig.15(a).

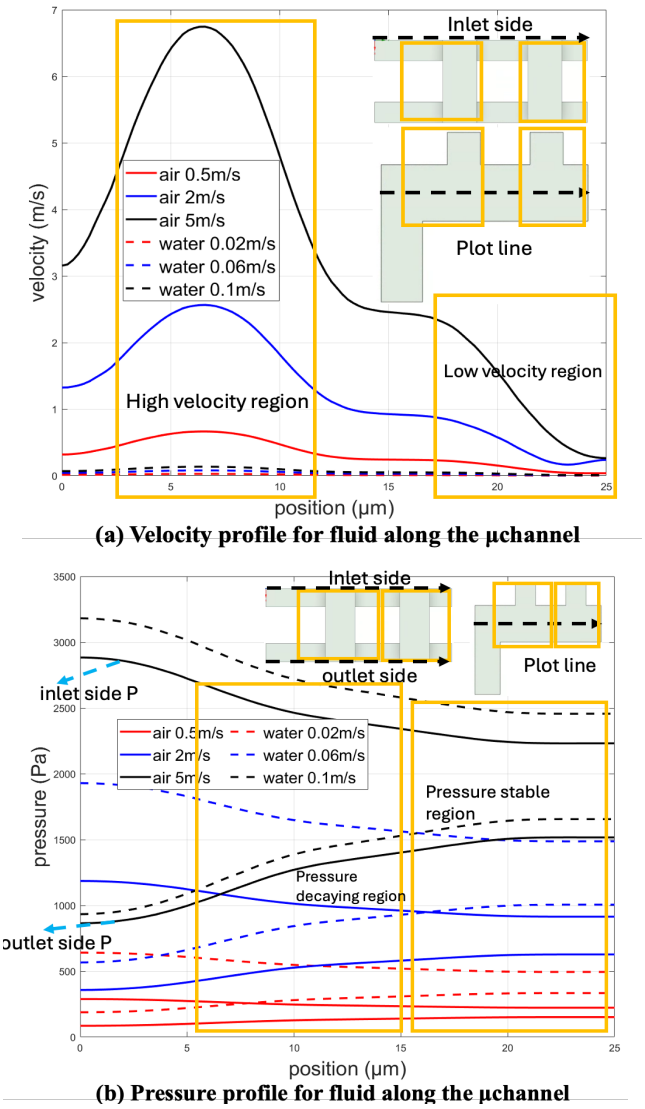


Figure 15: Water and air flow characteristics: (a) velocity magnitude profile along the fluid flow direction; (b) pressure profile along the fluid flow direction.

B. Unit cell model thermal analysis

The thermal performance is analyzed based on simulation results, and Fig.16 presents the temperature profile of the BSPDN chip unit cell model, using air cooling with a 5 m/s inlet as an example. The temperature profile indicates a significant temperature drop around the inlet region due to the substantial temperature difference between the chip's solid domain and the incoming flow. However, as the flow rapidly heats up, the heat dissipation rate sharply decreases after reaching the micro bump region. On the outlet side surfaces, the heat transfer conditions become more complex, and the overall heat transfer rate is negligible as the flow is heated to a temperature nearly identical to that of the nearby solid-fluid boundary surface.

A quick estimation for total microchannel heat extraction rate can be made by using equation $q=\dot{m}c\Delta T$ where q is the heat flow rate in W, $\dot{m}$ is the coolant mass low rate in kg/s, c is the specific heat of the flow in J/kg K, and ΔT is the temperature difference between flow inlet and outlet. For the case 'air cooling, inlet velocity=5 m/s', The heat flow rate q is calculated to be 3.26e-6 W. Also, the total heat flow from FEOL heat source is calculated to be 2.5e-4 W. Therefore, the estimated heat dissipation ratio for the case is only 1.3%, so the chip-top jet cooling still dominates the chip cooling. In contrast, for the simulation case 'water cooling with inlet velocity=0.1m/s', the heat dissipation ratio sharply rises to 34.1% by harnessing the same calculation approach. Therefore, it can be concluded that the microchannel air-cooling efficiency and cooling effectiveness are lower than that of microchannel water-cooling.

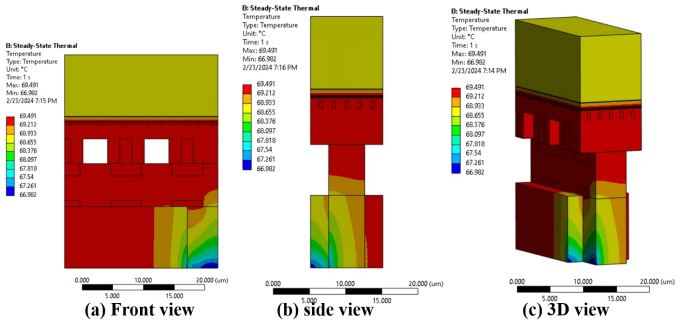


Figure 16: Temperature profile of the BSPDN chip solid region, air cooling, v =5m/s: (a) Front view; (b) side view; (c) 3D view.

The impact of a lower inlet temperature of 283K (10°C) on temperature is investigated alongside different coolant types and inlet flow velocities. The maximum temperatures in the Front-End of Line (FEOL) are illustrated in Fig.17. It is evident that water cooling can achieve a lower maximum temperature, whereas air cooling does not show a significant reduction. This can be attributed to water's superior heat removal ability as a coolant, given its four times higher heat capacity and 16 times higher mass flow rate compared to air, even under similar pressure drops. It is observed that reducing the inlet flow temperature from 300K to 283K can further decrease the maximum pressure. A 1.83% and 2.28% maximum temperature drop is observed for air cooling with a 2m/s inlet and air cooling with a 5m/s inlet, respectively. In contrast, the value sharply increases to 22.43% and 20.08% for water cooling with a 0.06m/s inlet and water cooling with a 0.1m/s inlet, respectively.

The temperature effect of a lower inlet temperature of 283K (10°C) is also investigated along with coolant type and inlet flow velocity. The maximum temperatures in the FEOL are illustrated in Fig.17. It shows that water cooling can achieve a lower maximum temperature whereas air cooling does not reduce it much, which can be explained by a better heat removal ability for water as coolant due to its 4 times higher heat capacity and 16 times higher mass flow rate compared to air, even under a similar pressure drop. It is observed that the maximum pressure can be further reduced by decreasing the inlet flow temperature from 300 K to 283 K. A 1.83% and 2.28% maximum temperature drop is observed for air cooling with 2 m/s inlet and air cooling with 5 m/s inlet, respectively, and the value sharply increased to 22.43% and 20.08% for water cooling with 0.06 m/s inlet and water cooling with 0.1 m/s inlet, respectively.

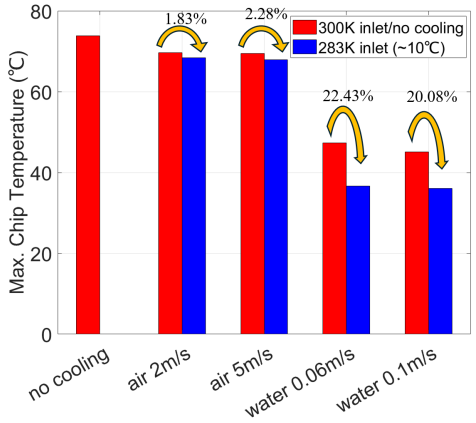
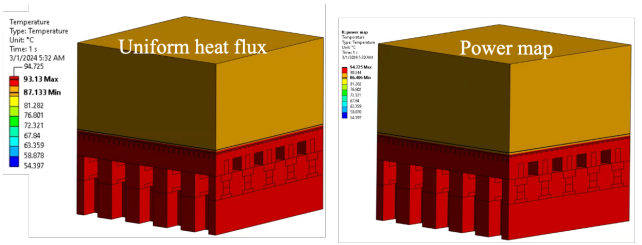


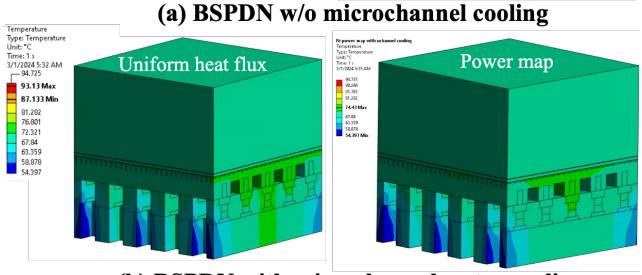
Figure 17: The maximum temperature in the BSPDN chip under different inlet flow conditions of distinct coolant, inlet flow velocity, and inlet flow temperature.

C. 50μm by 50μm modeling with Power map

The case 'water cooling with inlet velocity=0.06m/s ' of unit cell model is selected and its heat transfer coefficients for several surfaces are extracted using Newton's law of cooling $\dot{q}=h\Delta T$. These values are then applied to corresponding microchannel surfaces for the 50μm×50μm overall model. Both heat flux and temperature are extracted from unit cell model solid surfaces and temperature differences are calculated by subtracting this temperature by fluid temperature at very close position. It should be noted that the solid surfaces are separated to several sub-surfaces along the streamwise direction of inlet to well extract the non-uniformity of heat transfer coefficient. Surfaces on the outlet side are all set to be adiabatic since the overall heat transfer coefficient at that region is negligible due to high fluid temperature. Fig.18 illustrates the temperature distribution for all simulation cases.



(a) BSPDN w/o microchannel cooling



(b) BSPDN with microchannel water cooling

Figure 18: Temperature distribution for BSPDN chip solid domain under water coolant cooling, inlet velocity = 0.06 m/s: (a) Temperature distribution for chip without microchannel cooling; (b) Temperature distribution for chip with microchannel cooling.

Fig.19 gives values of maximum temperature on FEOL for all simulation cases. It shows that the maximum temperature for power map with and without microchannel cooling is 1.0°C and 1.6°C higher than that of uniform heat flux, respectively, given

that the average heat fluxes for heat source are kept the same. This is because the lateral heat spreading in FEOL, and thinned silicon substrate is constrained by their small thickness. Therefore, a nonuniform heat source can cause or deteriorate local hot spots, which increases the maximum temperature on FEOL. Maximum temperature drops of 21.17% and 21.43% are observed for uniform heat flux and power map by introducing microchannel cooling. However, it must be mentioned that, even though several sub-surfaces are used for heat transfer coefficient extraction to catch different local heat dissipation characteristics, there should be still modeling discrepancy because of the geometrical complexity and temperature dependence of heat transfer coefficient due to the heat spreading inside the geometry.

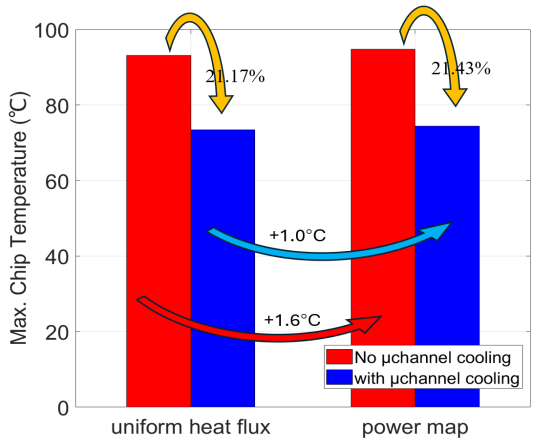


Figure 19: The maximum temperature for 50μm × 50μm overall thermal modelling with uniform FEOL heat flux or power map, with or w/o μchannel cooling. Water coolant, inlet velocity=0.06m/s, inlet temperature=300K.

V. Conclusions

In response to BSPDN thermal challenges, this study explores microchannel cooling for mitigating thermal issues within the BSPDN package structure using numerical modeling approach. The effective thermal conductivity of front side BEOL is studied to reduce the computation resource requirement for thermal modelling. Then, a unit cell model combining local BSPDN geometry and microchannel fluid domain is investigated by coupling steady-state thermal simulation with CFD, and ensure a co-convergence. Three variables, inlet velocity, inlet temperature, and coolant type, are set for control parameter study. The results show that water cooling, compared to air cooling, has higher cooling efficiency and effectiveness. After that, thermal performance of an overall model of size 50μm×50μm is studied with uniform heat flux or heat map on FEOL. Given the same average surface heat flux, the heat map leads to a higher maximum temperature due to local hot spot effect. To investigate the thermal influence of microchannel cooling, the effective heat transfer coefficients of case 'water cooling with 0.06m/s inlet' are extracted from several surfaces of the unit cell model to capture local heat dissipation features., which are then applied to the overall model for thermal numerical modeling. It shows that by harnessing the microchannel cooling, the BSPDN chip maximum temperature can be reduced by more than 20% or about 20℃ for both uniform heat flux and heat map cases.

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