Thermo-Mechanical Reliability Analysis and Raman Spectroscopy Characterization of Sub-micron Through Silicon Vias (TSVs) for Backside Power Delivery in 3D Interconnects

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***Abstract*—This study focuses on the fabrication and thermomechanical characterization of Through Silicon Vias (TSV) with diameters spanning 1-4 µm. In terms of TSV fabrication, scallop-free Si etching is achieved by the optimization of the Bosch etching process, and a void-free TSV filling is completed by a combination of electroless plating for seed layer and electroplating for TSV Cu filler. After that, the thermomechanical response of TSVs is stress-imaged via Raman spectroscopy. Thermal stress is developed in the Si after an annealing process at 400°C, which is attributed to the shrinkage of the Cu core as the sample cools down from the annealing temperature to room temperature. The stress profiles of TSVs with different diameters are measured and compared, revealing an equivalent stress level consistently below 100 MPa for all diameters. This lower stress level is attributed to the offset between tensile radial stress and compressive tangential stress. With the pitch fixed for different-sized TSVs, the interaction between adjacent TSVs is reduced for smaller TSVs, leading to a lower stress level and a transformation from single-peak to dual-peak stress distribution.**

Keywords—Heterogeneous integration, Through Silicon Via, Thermomechanical reliability, Raman spectroscopy

I. INTRODUCTION

"Monolithic 3D integration" using nanoscale interlayer vias (ILV) can achieve very high-density interconnections to support orders-of-magnitude energy and execution time improvements for future semiconductor technology nodes. This approach enables multiple layers of transistors (also referred to as active layers) and memory cells to be deposited sequentially—vertically on top of one another—and connected by short high-density interlayer vias (ILVs). The process temperature for each device layer fabrication is not compatible, however, requiring compromises in the thermal budget in fabricating each layer [1]. Alternatively, "Heterogeneous 3D integration" enables each thin device layer to be fabricated separately and then stacked vertically with each other using through-silicon vias (TSVs).

To capitalize on this heterogeneous approach while keeping pace with the continuous miniaturization of microelectronics, three-dimensional (3D) integration with fine-pitch and high-density interconnections is necessary [2]. TSVs must scale accordingly. TSVs have enabled several generations of high bandwidth memory (HBM) [3], which have become the must-have DRAMs for high-end, high-performance applications in graphics accelerators, network devices, datacenter AI ASICs, and FPGAs. The most widely used Cu-TSVs diameter in HBM and interposers is in the range of 5~10 µm. However, to meet the future high demand of memory density targeted at 100 GB/mm^2 to few TB/mm^2 [4], TSV interconnect size and spacing must be scaled down further to the submicron range (< 1 µm). Submicron TSV and microbump interconnects, for example, can enable ultra-high 3D interconnect densities reaching 1E+6/mm^2 to 1E+8/mm^2 for memory-on-logic stacking [5], [6], as illustrated in **Fig. 1**.

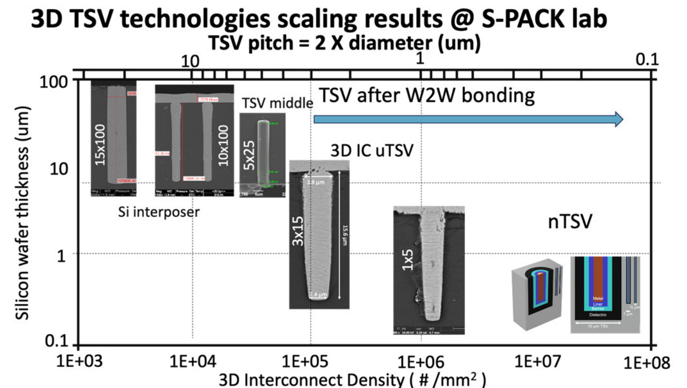

Figure 1 Future needs for high-density TSV interconnects [7], [8].

Nanoscale TSV are also a key enabler for the backside power delivery network (BS-PDN) [9], [10], [11], [12]. BS-PDN enables the power delivery to active devices from the backside by thinning wafers to nanoscale thicknesses and building up through-chip power transmission with nanoscale TSV. BS-PDN has shown great potential in advancing future semiconductor devices as it frees up space for signal routes and mitigates the IR drop. To accommodate the high density of transistors, TSV in the BS-PDN needs to be scaled down to sub-100 nm scale. However, such scaling presents serious challenges in the process development and material selection due to the aggressive scaling of via diameter.

Capitalizing on the advantages of TSVs and the heterogeneous integration that they enable requires pushing the technology from the microscale to the nanoscale and efforts have been invested to this end. **Table 1** lists the state-of-art research on ultra-small TSV diameter process with Cu, W, Co, and poly-Si as the TSV filler. Notably, a 110-nm via-last W TSV was demonstrated, with a height of 500 nm and an aspect ratio

of 4.5:1. A high aspect ratio Cu TSV for a 900 nm diameter was fabricated using a nano-Bosch silicon etching process with no scalloping. Besides Cu and W, an electroless Ni-TSV with a 500 nm diameter and an aspect ratio of 20 was also demonstrated. Taken together, the era of nanoscale TSV has arrived, and yet significant challenges remain as to how thermomechanical effects impact performance at these scales.

Table 1 State-of-art TSV dimensions reported in the literature.

Ref.	TSV diameter (μm)	TSV height (μm)	Aspect ratio (height/diameter)	TSV filler	Process
[12]	0.11	0.5	4.5:1	W	BEOL
[10]	0.18	0.5	2.7:1	W or Co	BEOL
[13]	0.5	10	20:1	Ni	BEOL
[14]	0.7	18	25:1	W/Poly-Si	FEOL
[15]	0.9	15	16:1	Cu	BEOL
[16]	1	10	10:1	Cu	BEOL
[17]	1.2	6	5:1	Cu	FEOL
[18]	2	45	22.5:1	W	FEOL
[19]	3	46	15.3:1	Cu	MEOL /BEOL
[20]	5	50	10:1	Cu	MEOL/ BEOL

II. CHALLENGES OF TSV SCALING

As illustrated in **Fig. 2**, the typical structure of TSVs consists of a metal core surrounded by two thin films, namely the barrier and the insulator. The TSV metal filling material could be W or poly-Si CVD-filled TSV for the via-first or via-middle process or electroplated Cu for the via-middle or via-last process. Beyond the central metal interconnect themselves, TSVs consist of both a dielectric layer to electrically isolate the metal from the silicon along with a barrier layer that limits the diffusion from the conducting metal to the dielectric. The liner layer is to improve the adhesion of the barrier and the central metal. Seed layers aiding in the deposition of these layers, meanwhile, are also present in this complex heterogeneous layered structure.

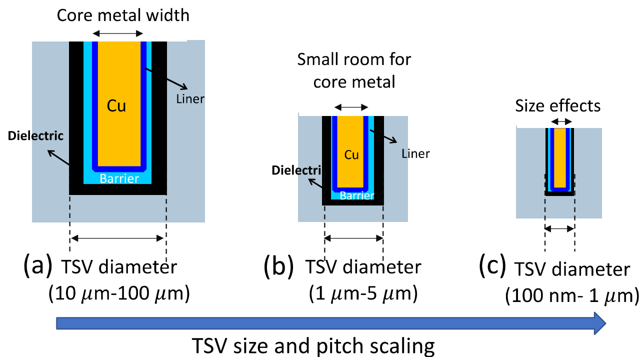

Figure 2 TSV diameter and pitch scaling from microscale to nanoscale. As the size of TSVs is scaled down to the sub-micron scale, the mechanical properties of the metal filling and the thin films can be affected by the nanoscale effects.

As we are pushing the scaling of the TSV diameter from 5 µm to 100 nm, the fabrications, including via etching, liner deposition as well as metallization become extremely challenging. For the high aspect ratio TSV via etching, a standard Bosch etching process uses alternative etching and deposition processes to create scallop-shaped sidewalls along the via. As the TSV diameter scales, the sidewall roughness becomes a more and more dominant factor for the via metallization. Therefore, a modified, scallop-free Bosch etching process has to be developed to minimize the sidewall roughness. For the TSV barrier and via filling, a conformal metal deposition is very critical due to the via shadow effects. Discontinuous barrier layer film deposition can result in metal diffusion into the Si or SiO_2 layer. Moreover, a nonconformal seed layer coating or discontinuous seed layer deposition can result in voids inside the sub-micron or nanoscale via [8].

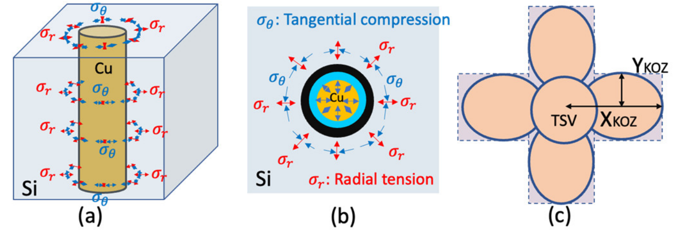

Figure 3 KOZ schematic of microscale TSV: (a) TSV induced radial and tangential mechanical stress 3D view; (b) top view of the TSV induced mechanical stress; (c) the KOZ area for single TSV configuration, illustrated the X_{KOZ} and Y_{KOZ}.

Scaling TSVs to the nanoscale presents not only fabrication challenges but also requires a sufficient understanding of the thermomechanical within the nanoscale TSV, which is a complicated heterogeneous system itself—as well as the surrounding silicon. With continuous scaling (see **Fig. 2),** TSV layers become smaller and thinner resulting in serious thermal and mechanical reliability concerns [21], [22], [23], [24]. The exact failure modes and interplay between the barrier, dielectric, and Cu layers when TSVs are subject to electrical, thermal and thermomechanical stress remains insufficiently understood. Scaling TSV technology to smaller sizes is not simply an exercise in driving the dimensions of existing processing techniques. Firstly, at these small scales, the materials act differently than their bulk counterparts. The mechanical properties, mass diffusion, and heat transport are each affected by size effects. For example, the shrinkage of the liner/barrier layer will lead to high line electrical resistance, resulting in an extra heat source for Joule heating. Furthermore, interfaces take on a heightened role as with smaller sizes the surface to volume ratio increases. The high thermal resistance of the thin barrier/liner layer will become the dominant factor for heat diffusion across TSV. The thermo-chemo-mechanical interplay among these differing layers, in turn, drives the stress existing within the TSV, electromigration, and ultimately the likelihood of their failure. It also dictates the stress within the adjacent silicon device layers and thus defines the so called “keep out zone” in **Fig. 3**, and the layout of the circuit itself [25]. To quantify the scaling of TSV technology, it is therefore necessary to identify first how the materials themselves change and only then how these changes ultimately influence TSV failure and strain within the active silicon layers.

The scaling of KOZ with TSVs is a topic that has been frequently addressed in the mesoscale, so too has the assessment of stresses within the TSV itself. Numerical solutions have assessed the impact of TSV: diameter, pitch, and

aspect ratio [25], [26], [27], [28]. Assuming purely elastic properties, the dependence of stress in the silicon and within the TSV only vary slightly [26]. Experimentally, optical—most often in the form of Raman spectroscopy—and electron (FIB based DIC) microscopy and diffraction methods have been used to quantify the stress within the silicon [29], [30], [31], [32]. These measurements have shown that elastic properties cannot account for the measured values of stress [30]. Rather, the stress state—and thus the KOZ—depends acutely on the plastic and viscoelastic properties of the copper, barrier, and dielectric layers. To date, however, studies examining the scaling behavior of nano TSVs have overwhelmingly focused on investigations employing elastic responses [27], [33].

The use of elastic properties in the analysis of nano TSVs is not without cause. Quantifying the viscoelastic, viscoplastic, and plastic response of materials is more difficult than their elastic counterparts. This is especially true in thin microelectronic layers where these properties can also become size dependent. For example, it has been shown that the yield strength of copper is significantly affected by the size of the layer [34]. Similarly, viscoelastic and viscoplastic effects primarily dictate the mechanical properties of SiO_2 [35], [36]. Simply put, the thin films making up the TSV are defined by non-elastic mechanical properties. These "non-linear" effects meanwhile, drive the stress state, film adhesion and thus the overall performance of scaling behavior of TSVs [37]. It is therefore necessary that any assessment of scaling and reliability of TSVs approach the problem with these non-linear, size-dependent, mechanical properties front and center.

In this study, we systematically investigate TSVs with diameters ranging from 1 µm to 4 µm through thermomechanical characterization and analysis. The fabrication process flow is developed for TSV test structures with an aspect ratio (AR) of 5:1. The TSVs are mechanically characterized after standard fabrication processes and thermal annealing. With those stress images, the effects of TSV diameter on the thermomechanical stress are studied, providing valuable insights for minimizing the impact of TSV-induced stress. The thermomechanical studies presented in this paper aim to establish a fundamental understanding of thermal stress in small-scale TSVs, facilitating the scaling down of TSVs to submicron-scale and nanoscale.

III. Fabrication of TSV

We developed the fabrication process for Cu TSVs with diameters ranging from 1 µm to 4 µm and an aspect ratio of 5:1. The fabrication process flow for the Cu TSVs is shown in **Fig. 4**, including patterning, etching, thin film deposition, electroplating, polishing, and stress imaging.

The TSVs are first patterned with optical lithography. An array of circular holes with a pitch of $p = 10$ µm is patterned with photoresist on a silicon wafer with 200-nm SiO_2. AZ1518 is spin-coated at 4000 rpm to achieve a targeted photoresist thickness of 1.8 µm. The wafer is pre-baked at 100 °C and exposed with a Heidelberg MLA 150 maskless aligner using a 405 nm laser. The exposed wafer is developed in MF-26A developer and hard-baked at 110°C to achieve optimal resistivity to the plasma etching.

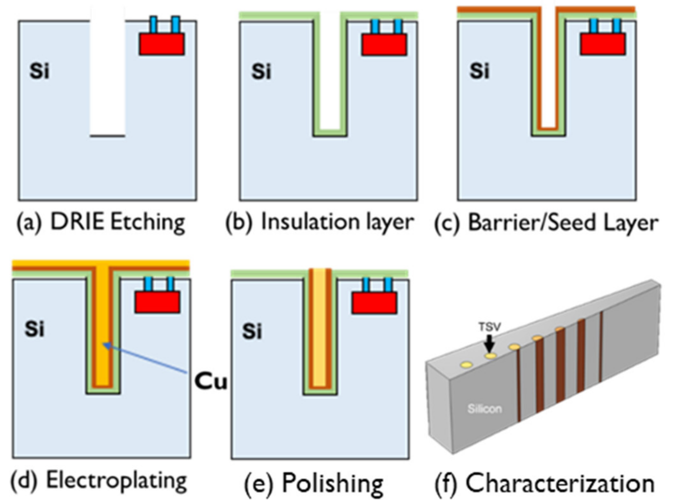

Figure 4 Process steps for the formation of TSV testing structure. A process flow containing (a) Deep reactive ion etching (DRIE), (b) Plasma-enhanced chemical vapor deposition (PECVD), (c) Physical vapor deposition (PVD), (d) Cu plating, (e) CMP, and (f) Raman spectroscopy is developed.

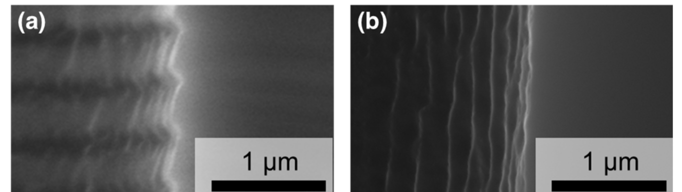

Figure 5 Comparison of sidewall roughness of Si vias etched with the Bosch process. (a) Before optimization. (b) After optimization.

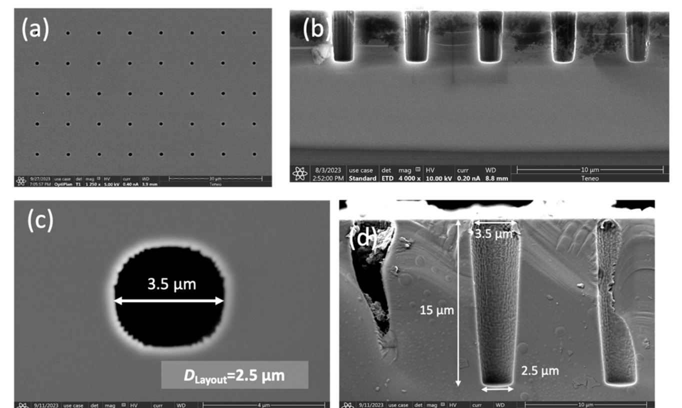

Figure 6 Via etching for small scale TSV diameter (a)(b) 1-µm via etching optimization. (c)(d) Etched via with a diameter of 3 µm.

The SiO_2 layer is then patterned with a reactive ion etching (RIE) tool and serves as the hard mask for Si etching. The deep Si vias are formed with the Bosch process, which etches deep vias with vertical sidewalls by switching between the etching (SF_6/O_2) and deposition (C_4F_8) processes. A process optimization is performed on the Si etching process to achieve a scallop-free via etching. By increasing the switching frequency and adjusting the etching/deposition power, we develop a deep Si etching process with a smooth sidewall. The SEM images in **Fig. 5** show the improvement of sidewall roughness after

process optimization. **Fig. 6** depicts Si vias with diameters down to 1 µm.

A thin SiO_2 insulation layer is then deposited to provide electrical insulation for TSVs. A 60-nm SiO_2 film is deposited at 170°C with a Plasma-Therm high-density plasma chemical vapor deposition (HDPCVD) tool. The thickness of SiO_2 is examined with a thin-film mapper to validate the process and assess the uniformity of SiO_2 deposition. A thickness variation of +/− 2% is demonstrated, ensuring a uniform coverage of the insulator on the wafer.

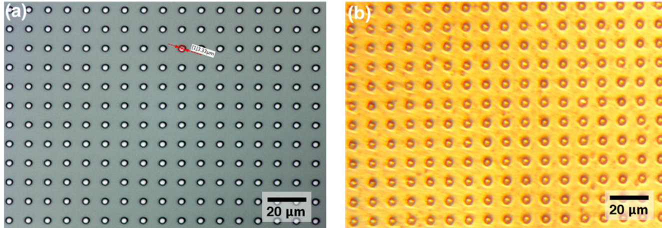

Figure 7 Electroplating of 3-µm TSVs. (a) Via patterned with lithography. (b) Microscope image of Cu electroplated TSVs.

A 30-nm Ti and a 300-nm Cu thin film is deposited with a physical vapor deposition (PVD) sputtering tool to create a barrier and a seed layer on the side wall and top surface of the TSV. The via is electroplated to achieve TSV metallization. The sample is pre-wetted in a vacuum chamber with DI water to extract air bubbles. A Cu electroplating solution with additives, including suppressor, leveler, and accelerator, is used as the plating base. The TSVs are then plated with a 0.1 ASD DC to achieve high-quality TSV filling. The top-view optical image in **Fig. 7** shows the TSV array filled with copper. However, insufficient sputtering power and film thickness can lead to poor coverage of the seed layer and result in a large void near the bottom of the via. **Fig. 8(a)** shows TSVs with voids caused by the discontinuity of the seed layer.

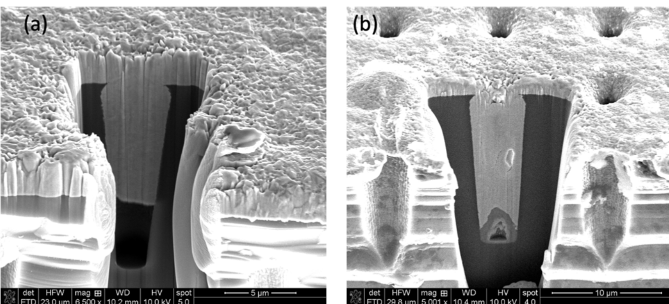

Figure 8 Void formed due to the poor coverage of the seed layer. (a) FIB image of a TSV with a large void at the bottom. (b) Improved metal filling with a short time electroless plating.

To improve the continuity of the Cu seed layer, a 100-nm electroless plated Cu is deposited before electroplating. The electroless Cu improves the continuity of the seed layer and eliminates the void at the bottom of TSVs. The cross-section SEM images of the TSVs in **Fig. 8 (b)** shows the improvement of via filling with a short time electroless plating. The electroless plating process is further optimized and combined with prewetting methods to create a high-quality metal filling of TSVs. The high yield TSV Cu filling is shown in **Figs. 9** and **10**.

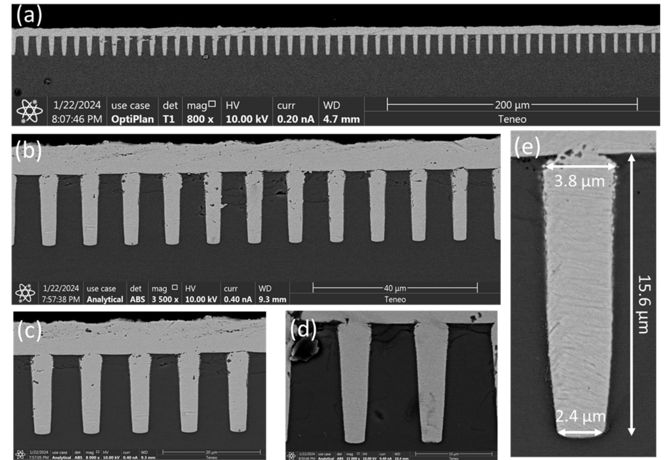

Figure 9 SEM images showing the cross-sections for 3-4 µm TSV with high yield.

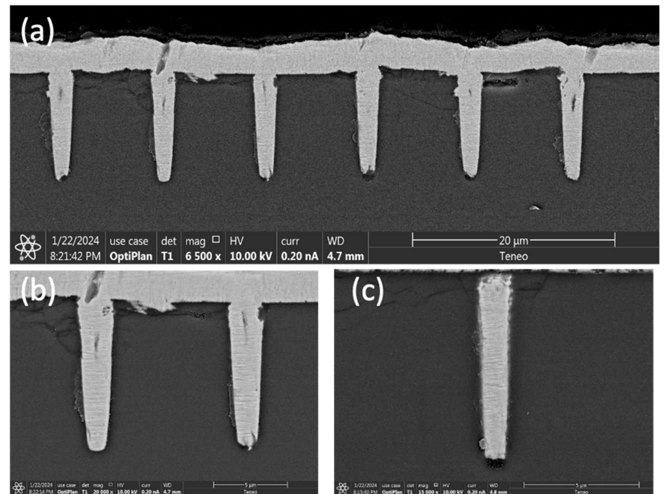

Figure 10 SEM images showing the cross-sections for 1-2 µm TSV with high yield.

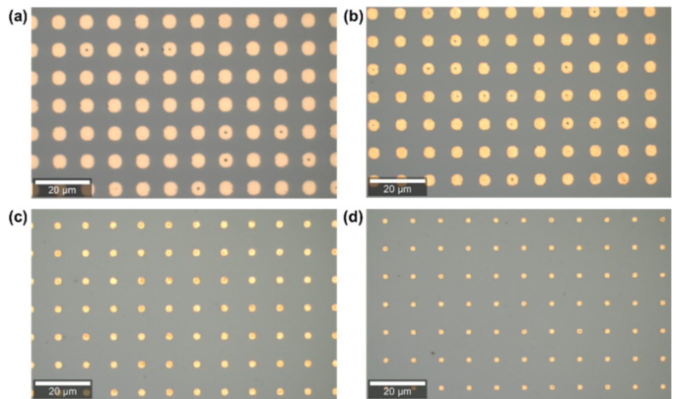

Figure 11 Polished top view of TSVs with a diameter of (a) 4 µm, (b) 3 µm, (c) 2 µm, and (d) 1 µm. The pitch of the via array is fixed at p = 10 µm for all the diameters.

After electroplating, a CMP process is performed to remove the excessive copper on the top surface of the sample. The top

view of the polished TSV samples is inspected with an optical microscopy system and is shown in **Fig. 11**.

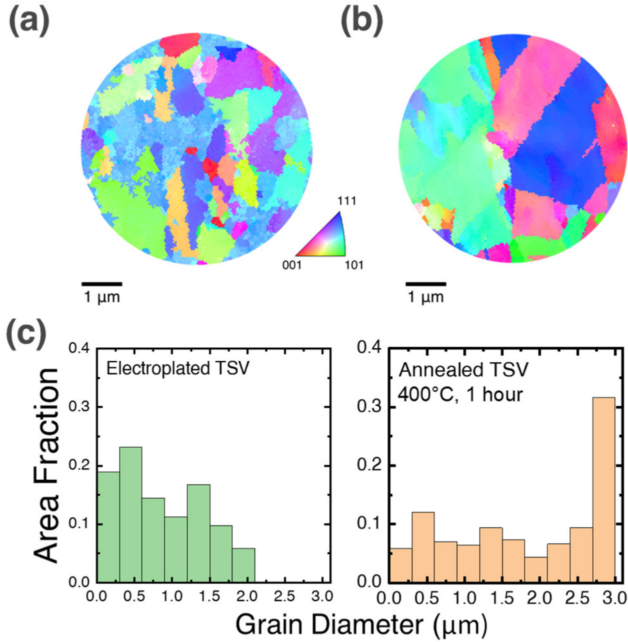

Figure 12. EBSD images showing Cu grain of a 4-μm TSV before and after annealing. Grain orientation mapping of (a) TSV with Cu electroplating and (b) TSV annealed at 400°C for 1 hour. (c) Variation of grain size due to annealing.

To stabilize the microstructure of the Cu TSVs, a high-temperature thermal annealing process is applied after the CMP process [38]. In this paper, we selected a common annealing condition (400°C, 1 hour) to evaluate the thermal stress induced by the annealing process. The annealing process is performed in a high-temperature furnace. Forming gas containing 96% N_2 and 4% H_2 is purged into the furnace to avoid the oxidation of copper.

The grain size of TSVs before and after annealing is assessed with an EBSD detector in SEM. As shown in **Fig. 12**, the grain size of the TSV significantly increased after annealing. It is also worth noting that the grain size is smaller than those reported for TSVs with same annealing condition but larger diameters [39]. Given that the mechanical behavior of copper has been demonstrated to be affected by the grain size [40], the dependence of grain size on TSV diameters can change the mechanical properties of Cu core, leading to size-dependent thermomechanical response of TSVs at the sub-micron scale.

IV. Raman stress measurement

The TSVs are then characterized with Raman spectroscopy to image the stress distribution. A Witec Alpha300 Raman spectrometer is used with a laser wavelength of 532 nm and a laser power of 0.5 mW. A piece of bare silicon is taken as the stress-free reference. The Raman shift is measured for the Si part of the TSV sample and compared with the stress-free sample to evaluate the equivalent stress near the top surface of Si. The correlation between the Raman shift and the equivalent stress can be expressed as

$$\omega - \omega_0 = D\left(\sigma_{rr} + \sigma_{\theta\theta}\right) \quad (1)$$

where $\omega - \omega_0$ is the frequency shift in cm^{-1} with respect to the stress-free sample, σ_{rr} and $\sigma_{\theta\theta}$ are the radial and tangential stresses, and D is a pre-factor and has been determined as D = 3.6 cm^{-1}/GPa for Raman backscattering from the (001) surface of silicon [41].

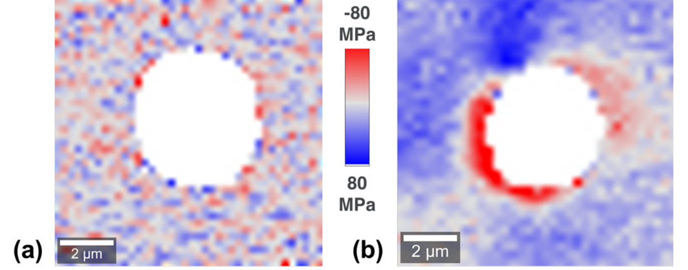

Figure 13. 2D map showing the thermal stress distribution induced by a 4-μm TSV. (a) Before thermal annealing. (b) After being annealed at 400°C for 1 hour.

Before annealing, the background stress in Si is first scanned with Raman spectroscopy. Considering that all the Cu electroplating process is performed at room temperature, the Cu TSVs will not expand or shrink without heat treatment. Therefore, the sample is expected to be close to the stress-free state before annealing. As shown in **Fig. 13(a)**, the stress was imaged on the silicon substrate near a 4-μm Cu TSV without any heat treatment. No significant stress concentration is observed, and the stress level is smaller than 20 MPa. A line scan is performed with a higher integration time and lower uncertainty to further confirm the stress distribution. The Raman shift is measured on a horizontal line through the center of TSVs at different diameters ranging from 1 μm to 3 μm, and the stresses are evaluated at a 200-nm pitch. As depicted in **Fig. 14**, the equivalent stress is found to be lower than 15 MPa for all three samples, and the impact of Cu TSVs on the stress distribution is insignificant.

The TSV samples are then annealed at 400°C and imaged again with Raman spectroscopy. **Fig. 13(b)** shows the stress profile near an annealed 4-μm TSV. The concentration of compressive stress is observed near the TSV. The detailed distribution of equivalent stress is revealed with a line scan. As depicted in **Fig. 15**, annealed TSVs with different diameters are mechanically characterized by Raman spectroscopy. The equivalent stress is found to be compressible near the copper TSV and increases to the tensile state as the measured location moves away from the Cu core, aligning with the stress imaging result.

The equivalent stress is lower than 100 MPa for all the annealed samples. The small stress level can be explained by the opposite signs of the radial and tangential stresses. As the sample is cooling down from the annealing condition to room temperature, the Cu TSV shrinks against the Si substrate, leading to tensile radial stress and compressive tangential stress. The offsets between radial and tangential stress lead to a small level of equivalent Si stress. A similar phenomenon is observed

by Ryu et al. [42] in their previous study on the thermomechanical stress induced by 10-μm TSVs.

Comparing the thermal stress induced by TSVs with different diameters, it can be concluded that as the size of TSVs decreases, the peak stress level also decreases. As depicted in **Fig. 15(a)**, the single stress peak between 3-μm TSVs illustrates a strong interaction between the two Cu cores. The stresses induced by the two adjacent 3-μm TSVs overlap with each other and contribute to a larger stress in the TSV array. However, the stress profile for smaller TSVs, such as the 2-μm and 1-μm TSVs in **Figs. 15(b)** and **15(c)**, show a distinctive dual-peak pattern, which can be attributed to the weaker interaction between TSVs. With the pitch fixed, the spacing between the vias becomes larger as the TSV diameter increases, leading to a weaker interaction between adjacent TSVs. In addition, the area affected by a single TSV can decrease at smaller diameters, further diminishing the interactions between small-sized TSVs.

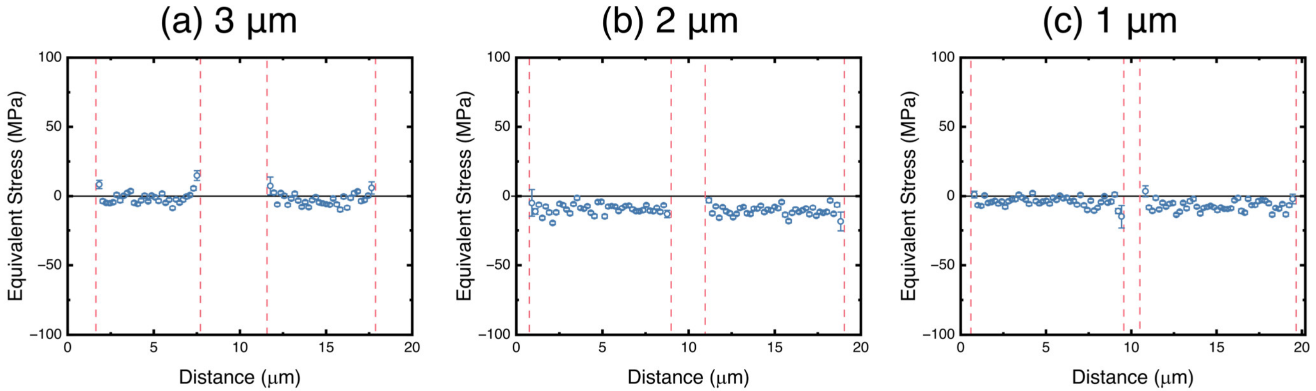

Figure 14. Line scan through the center of the TSVs showing the distribution of equivalent stress before annealing. TSVs with a diameter of (a) 3 μm, (b) 2 μm, and (c) 1 μm are investigated.

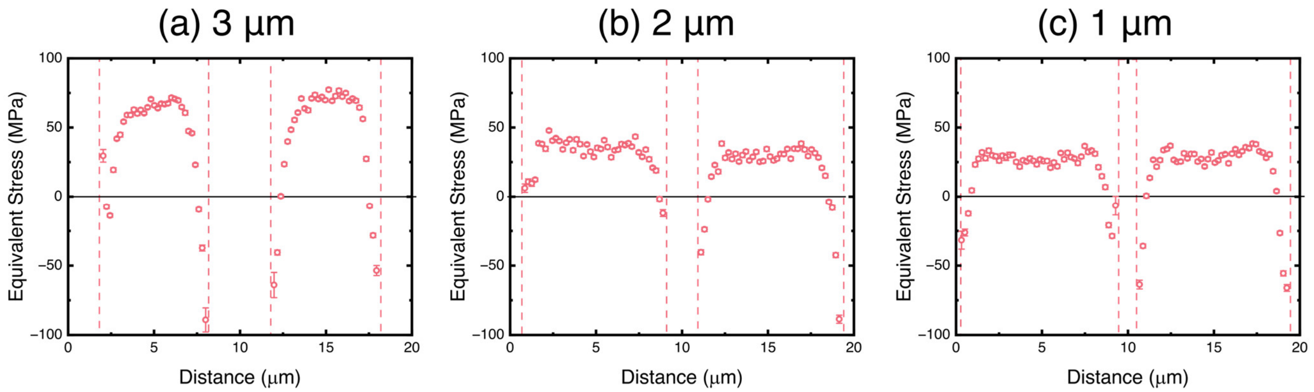

Figure 15. Line scan through the center of the TSVs showing the distribution of equivalent stress after being annealed at 400°C for 1 hour. TSVs with a diameter of (a) 3 μm, (b) 2 μm, and (c) 1 μm are investigated.

CONCLUSIONS

In this paper, we demonstrate the fabrication process flow for TSVs with scallop-free etching and void-free metal filling. An aspect ratio of 5:1 and diameters down to 1 μm are achieved. With Raman spectroscopy, the thermomechanical response of different-sized TSVs is measured and analyzed. The main conclusions are as follows:

1. A scallop-free silicon etching is developed for TSVs down to sub-micron scale. The roughness of the sidewall is significantly reduced with the optimized Bosch process.
2. Cu seed layer deposited with PVD sputtering can be insufficient for sub-micron scale TSVs. An electroless plating process is applied for seed layer enhancement. With a low current density DC electroplating, a void-free TSV filling is achieved.
3. The thermal annealing process increases the Cu grain size for TSVs but leads to significant thermal stress in the silicon substrate. The equivalent stress is found to be compressive near the TSVs and tensile at locations away from the TSVs after being thermally annealed at 400°C for 1 hour.
4. A single-peak stress profile is found between 3-μm TSVs. As the TSV scaled down, the larger spacing and smaller affected area of Cu cores reduces the interaction between two adjacent TSVs, leading to a smaller stress level and a distinctive dual-peak stress pattern.

Acknowledgment

This work is supported by the Semiconductor Research Corporation (SRC), as a part of the Global Research Collaboration (GRC) in the Center for Heterogeneous Integration Research on Packaging (CHIRP). We thank our SRC liaisons, including Yu-Tao Yang from MediaTek and Se-Ho You from Samsung, for their feedback and input.

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