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Parametric design analysis of a multi-level 3D manifolded microchannel cooler via reduced order numerical modeling

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ABSTRACT

Waste heat flux from power dense electronics is expected to reach > 1 kW/cm^2 in the next few decades, and they will require novel cooler designs with low thermal resistance, that can simultaneously dissipate large levels of heat and have high coefficient of performance (COP). 2D straight microchannel cold plates (CP) are an industrial go-to solution for active heat dissipation needs, but they suffer from a major drawback – very high pump pressure is required to force large quantities of fluid through miniscule channels in the CP and thus these coolers are very inefficient, achieving low COP. Recently, manifolded micro-coolers (MMC) have become popular which use a second manifold layer to distribute the fluid in 3D within the CP, thus shortening fluid travel length within the miniscule CP channels and significantly reducing the total device pressure drop. In this study, we first introduce a novel two-level manifold design which boasts a potential of > 2x improvement in COP compared to conventional single-level manifold concept without affecting the thermal performance. Recognizing the difficulty in simulating large area full MMCs, we then aim to simplify the 2-level MMC geometry into reduced order models to bring down simulation cost at an expense of accuracy. Two models were considered, the widely popular and convenient to use Single Cold Plate U-bend Channel (SCPUC) model which only simulates the CP channels, and the slightly more complicated Single Manifold Channel (SMC) model which also considers the effect of the manifold. The SMC model simulations were first validated against full device simulations for different heater footprint sizes (25, 100, 400 mm^2) to establish accuracy and it was found that the SMC model could predict thermal performances of all device sizes with a nominal inaccuracy of 5%. In contrast, the widely accepted SCPUC model produced highly inaccurate (as high as 25–45%) predictions for thermal performance of the MMCs. The two models were then used under an extreme heat flux load of 800 W/cm^2 and 0.2 liter per min (lpm) device flow rate, to simulate 54 different 2-level MMCs obtained by varying important geometric parameters on the manifold and cold plate side. Detailed analysis was performed to explain the trends in thermal performance and pressure drop with different geometric parameters. Finally, two pareto curves were reported, one between thermal resistance and pressure drop, and the other between COP and device size. It was seen that the proposed 2-level MMC showed record high COP as compared to state-of-the-art single-level MMCs. We hope that this study will act as a design guide for MMCs as well as act as a performance repository for a wide range and combinations of geometries of 2-level manifold structures.

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Nomenclature

Symbol	Nomenclature	Unit
$2D$	2 dimensional	–
$3D$	3 dimensional	–
A	area*	m^2
α	CP channel aspect ratio	–
BC	boundary condition	–
CFD	computational fluid dynamics	–
CHF	critical heat flux	W/cm^2
COP	coefficient of performance	–
CP	cold plate*	–
C_p	specific heat capacity	$J/kg-K$
$CP_{thickness}$	thickness o cold plate layer	μm
$EMMC$	embedded manifolded micro-cooler	–
h	heat transfer coefficient*	W/m^2K
H	height*	μm
k	thermal conductivity*	W/mK
L	length of heated zone*	mm
L_c	characteristic length of a simple fin problem	mm
$\dot{m}$	mass flux*	kg/s
MF	manifold*	–
$MF_{thickness}$	thickness of Manifold layer	μm
MMC	manifolded micro-cooler	–
μ	viscosity	$Pa-s$
n	number of channels*	–
Nu	Nusselt number	–
P	pressure*	Pa or kPa
P_m	perimeter	mm
ΔP	pressure drop*	Pa or kPa
q''	heat flux	W/cm^2
r	direction vector*	m
R	thermal resistance total*	K/W
R''	area normalized resistance defined based on heat flux*	cm^2-K/W
Re	Reynolds number*	–
ρ	density	kg/m^3
$SCPUC$	single cold plate channel U-bend channel	–
SMC	single manifold channel	–
T	temperature*	K
TIM	thermal interface material	–
u	velocity*	m/s
W	width*	μm
x	power law exponent in $Nu-Re$ relationship	–

* These variables or abbreviations have been used by themselves and sometimes with additional subscripts as well in the main text, the subscripts provide additional detail.

1. Introduction

Continued pursuit for faster and better performance from electronic devices have prompted researchers to pack power dense transistors like MOSFETs, IGBTs etc closely together. Such tight packages with high volume density of transistors not only lead to superior device performance but also an exponential rise in waste heat generation. Wide Band Gap SiC and GaN based devices, power inverters, AC-DC converters, next generation compute technologies (GPU, TPUs), electric vehicles, renewable power generation, high frequency radar are some of the current technologies that already produce waste heat flux of 50–150 W/cm^2 with heat dissipation level projected to reach 1000 W/cm^2 in the near future [1]. Furthermore, researchers are envisioning 3D chip stacked architecture to replace conventional 2D microchips to keep up with the prediction of Moore's Law to further improve device metrics, thus further exacerbating the heat management problems. Therefore, industry today faces an urgent need for development of aggressive, large area heat management solutions and their integration with existing technology, which will keep the device operating temperatures low, improve device efficiency and performance, prevent thermal degradation and cycling issues, increase device longevity and promote safety.

One of the pioneering works by Tuckerman and Pease showed the potential of embedded microchannel for chip-cooling [2]. A Cold Plate (CP) with straight 2D microchannels (1 mm long, 57 μm wide) was used to dissipate extreme heat flux of 790 W/cm^2, although with a very high device pressure drop (ΔP) of 215 kPa, which was a result of forcing large quantities of water through miniscule microscale channels. This is extremely undesirable since large ΔP would lead to low coefficient of performance (COP) and require bulky pump hardware to be integrated in the flow system. Severe space constraints in high power electronic packages restrict the use of these large flow components, thus preventing widespread commercial adoption of such microcoolers with high pressure loss (> 50 kPa). This issue can be mitigated effectively using a second fluid distribution layer on top of the microchannel CP called the manifold (MF). This layer aims to route the fluid in a 3D top-down fashion, thus shortening fluid travel length within the CP and reducing pumping power required while simultaneously maintaining superior thermal performance levels. As early as 1991, Harpole and Eninger predicted by theoretical modeling the ability to achieve, at the time, a whopping 10 W/cm^2-K heat transfer coefficient by using Manifolded Microcoolers (MMC), and thus being able to cool > 1 kW/cm^2 with a sensible heat rise of 30 °C at 101 kPa device ΔP [3].

Since then, the superior thermal performance of MMC designs have been experimentally investigated by several studies [3–7,8], all of which demonstrated extreme heat flux (~1 kW/cm^2) removal ability by leveraging the high heat transfer coefficients associated with phase change flow of liquid coolants in tiny microchannels of the MMC. However, two-phase flow in microchannels is also inherently accompanied by large ΔP (> 100 kPa) caused by the expanding vapor in the channels, and therefore again needing bulky pump components which severely limit its application space. Cetegen removed 1.23 kW/cm^2 heat flux using R-245fa from his forced fed microchannel heat sink (FFMHS) with 60 kPa pressure loss [4]. Back et al. [5] and Drummond et al. [6] used HFE-7100 in a complex 8-chip stack manifolded cooler to remove 660 and 910 W/cm^2 of heat flux at high pressure losses of 138 and 162 kPa respectively. van Erp et al. [7] even went on to build a manifolded cooler directly at the back of a high power AlGaN/GaN Schottky diode a.c.-d.c. converter to show that a massive, 1.7 kW/cm2 heat flux can be removed using water at a ΔP of 130 kPa. Alongside the high ΔP issue, two-phase microchannel flows are also marred by other severely prohibitive reliability problems like, rapid bubble growth instability, Ledinegg instability, parallel channel instability, upstream compressible volume instability [9]. These instabilities tend to set in abruptly during device operation and are extremely difficult to predict and suppress, thus, they often lead to sudden, chaotic fluctuations in device pressures and flows, drastic reduction in safely removable critical heat flux (CHF), and ultimately device failure. These issues have prevented the widespread use and commercialization of active two-phase cooling solutions, with almost all existing commercial coolers being single-phase. Single Phase coolers suffer from a different challenge – since it unable to leverage the extremely high heat transfer coefficient characteristic of boiling and two-phase flows, the maximum heat flux that can be dissipated by a single-phase cooler at low ΔP (< 50 kPa) is also significantly reduced. Everhart forced large quantities of water through an EMMC device to remove 622 W/cm^2, although at a much high ΔP of 138 kPa [10]. Other studies there were able to keep ΔP levels low, also suffered a massive hit in the critical heat flux dissipated. Back et al. [5] and Drummond et al. [6] reported heat flux dissipation levels of 100–175 W/cm^2 using single phase operation of HFE-7100. Escher used water to remove 100 W/cm^2 from a larger area (400 mm^2) manifolded cooler [11]. Cetegen optimized surface, S17 could achieve up to 250 W/cm^2 flux removal using single phase operation of R-245fa. Boteler et al. showed a record 331 W/cm^2 heat flux removal by forcing single phase water through their EMMC at significantly lower ΔP of 38.6 kPa [4]. Boteler et al. also investigated their cooler design through CFD sim-

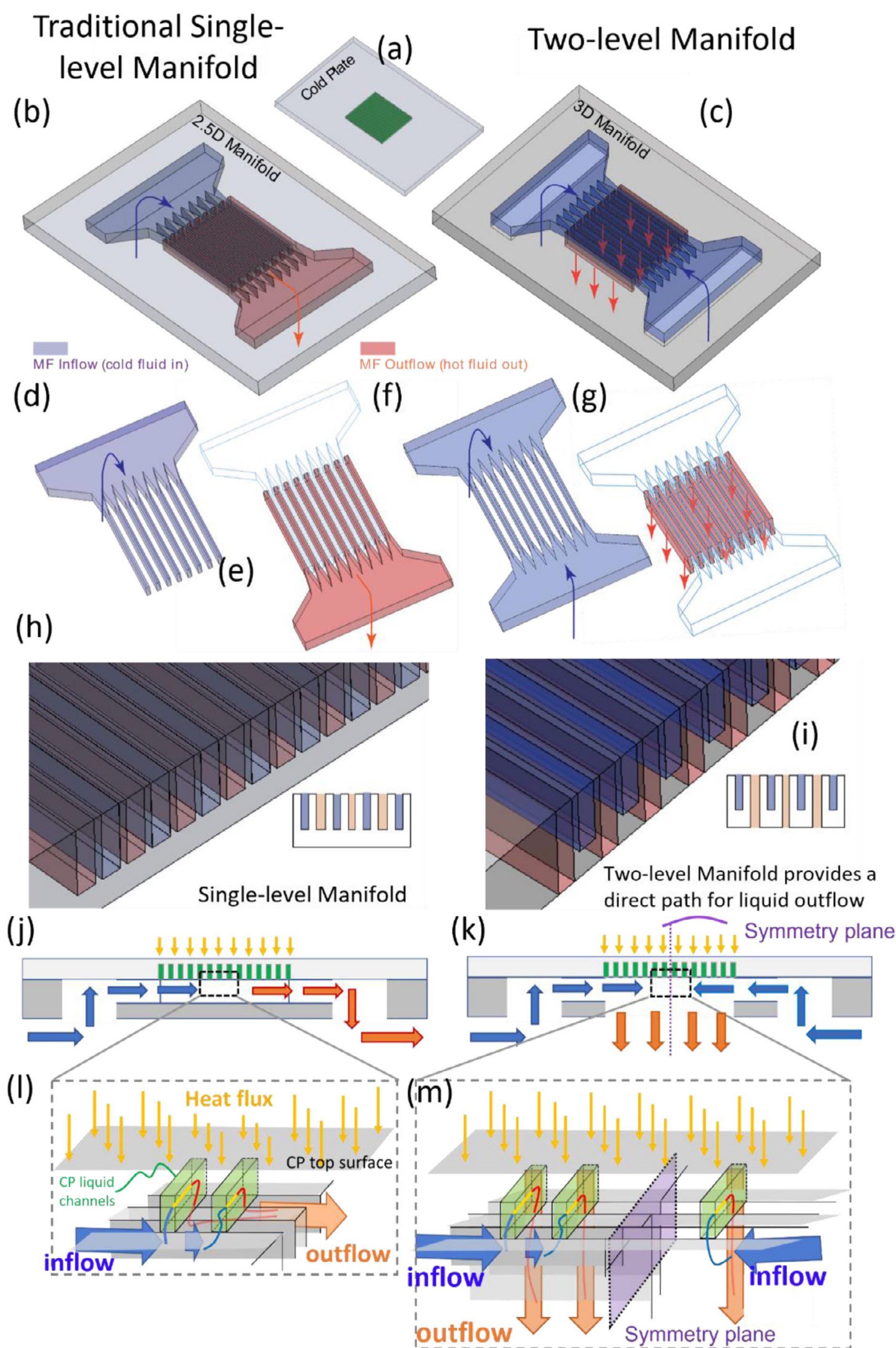

Fig. 1. (a) Cold Plate (CP) – with channels (green) going from left to right, this serves as the active site for heat transfer between chip heat flux and coolant fluid flow, (b) Conventional single-level Manifold with one inlet and one outlet on either side of the heater section, (c) 2-level Manifold showing two inlets on two sides and a normally oriented outlet through the wafer, (d) Inflowing cold fluid fills the blue section and (e) outflowing hot fluid fills up the orange section of the single-level-MMC, (f) Inflow (blue) and (g) Outflow (orange) sections in a 2-level MMC, (h) cross-section of a single-level Manifold, (i) cross-section of a 2-level Manifold, (j,k) Cross sectional view of fluid flow and heat transfer in a (j) single-level MMC and (k) 2-level MMC, (l,m) Fluid flow from MF inlet to MF outlet via CP channel bridges in a (l) single-level MMC and (m) 2-level MMC.

ulations, and identified the potential to remove 400 W/cm2 of heat flux while still operating the device in the single-phase regime using their cooler configuration [12]. Thus, continued effort keeps getting directed towards realizing innovative EMMC designs with efficient flow paths and geometries that aim to push the limits of COP (achieved by coolers with high heat flux removal capability and simultaneously very low device ΔP) while being able to remove extreme (> 500 W/cm2) levels of heat flux using only single-phase flow of coolants.

Recently, it has been seen that the manifold design can be further optimized from being conventional single level [12,13,14] (Fig. 1 left side) to being multi-level (Fig. 1 right side) [15–17]. These multi-level manifolds are attractive because they can lower the flow path within the EMMC device by > 50% as compared to their conventional single-level counterparts [12,13], thereby enabling further reduction in ΔP and increase in COP, at similar levels of thermal performance. Because of challenges associated with making multi-level structures using conventional lithography

techniques, most manifolds in EMMCs discussed above are designed to be single-level structures – where the inlets and outlets are at the same level in a wafer. However, recently, Hazra et al. [15] detailed a double-sided processing flow coupled with a novel, anisotropic, deep Si reactive ion etching technique that can create multi-level large area (> 600 mm^2) manifold structures with nominal feature dimension ~ 10 μm, reliably and repeatably – a finding that will encourage wide-spread adoption of two-level manifold structures for extreme heat flux cooling devices. Furthermore, Jung et al. [18] used single phase flow of water in such a 2-level MMC to remove a tremendous 300 W/cm2 of heat flux at a negligible ΔP of mere 3 kPa. The use of single-phase water for device operation is accompanied by another boon – the ability to easily model the thermofluidic performance of these devices through CFD with great accuracy. Jung et al. performed numerical simulations of his 3DMM cooler and showed that simulation results corresponding to forced fed single-phase operation of water matched very closely to that of experiments performed within an uncertainty range of ± 10% [17,18]. The promise of superior heat removal performance over large areas with record low input power (ΔP) makes these 2-level 3DMMC type designs ideal for successful scale up, which was not possible for other existing conventional single-level manifolded coolers beyond 100 mm^2 because of the comparatively higher ΔP associated with single-level manifolds. Piazza et al. [16] performed numerical simulations of a 3DMMC design as its heater footprint increased from 25 to 400 mm^2, to show that superior levels of thermal performance characteristic of the smaller 25 mm^2 devices can be achieved by the larger 3DMMC too, albeit with an additional ΔP penalty of 10–100 kPa. This study simultaneously revealed one major, but well known [16,14,19–26] challenge in numerical simulation of large area 3DMMCs associated with the exponentially increasing cost of simulation with increased device footprint area – a major deterrent to research and development of high-performance large area 3D MMC coolers.

Wang and Ding [27], Boteler et al. [13] and Yang and Bing-Yang [8] could successfully perform full device simulations on MMCs with only a small number (2–30) of channels. Jung et al. [17] and Piazza et al. [16] employed the inherent symmetry in their device to perform quarter (1/4th) model simulations which helped marginally reduce simulation cost. This high cost is associated with exponentially larger number of mesh elements required to satisfactorily resolve the CP channels (as small as 10–50 μm) as the device size increases – a problem that becomes so severe at > 400 mm^2 device footprint or for small CP channel widths < 50 μm, that full or 1/4th device simulation becomes impossible. Thus, in recent times, research has burgeoned into mitigating this exorbitant cost issue that has been plaguing the use of numerical simulations tools as a pre-manufacturing step for rapid design optimization of large sized EMMCs. Escher et al. [28] and Sarangi et al. [19] simplified the difficult to mesh CP channels with a porous media approximation, an approach that led to lower simulation expense at the cost of accuracy. However, this method when applied to 3D manifolds fails to capture the non-uniform fluid distribution induced by the manifold among the Cold Plate channels and we lose important information about the detailed temperature map at the junction between the Cold plate and heat producing chips. A very common approach by several prior studies like ones by Cetegen [4], Arie et al. [14], Copeland et al. [20], Poh and Ng [21,22], Lee et al. [23], Husain and Kim [24], Mandel et al. [25], Sarangi et al. [19] and Ryu et al. [26] is to ignore the manifold altogether, setting up a much simpler CP channel model. This model only considers flow in the u-bend section that is formed by a short section of the CP channel connecting a set of adjacent MF inlet and outlet channels with the simplifying assumptions that the MF distributes the fluid somewhat uniformly across all the CP channel bridges. This model was widely adopted because it is simple and could be easily parametrized using conventional CFD packages like ANSYS, which enabled fully automatic rapid simulations. The ability to simulate, automatically and quickly, a wide range of parameters, under different flow and heating scenarios further led to significant research in simulation driven optimization, modeling, and flow pattern analysis of such EMM coolers. Only very recently, it has been suggested by Boteler et al. [13] and Arie et al. [14] that these CP only models are extremely error prone, that strong thermofluidic coupling exists between the MF and the CP in manifolded coolers, which necessitates that we consider the effect of manifold in our simulations as well. Boteler indicated a 56% underestimation of heat transfer coefficient in the simplified u-bend CP channel model as compared to that achieved after including the manifold to the simulation.

In this study, we first introduce the concept and design of a novel multi-level MMC design similar to one briefly investigated upon experimentally by Jung et al. [18] and later numerically by Piazza et al. [16] and Jung et al. [17]. This multi-level manifolded cooler design with a smaller flow path length is then theoretically compared with conventional single-level manifolded coolers with comparatively longer device flow path, to understand the effect of device scale up on thermofluidic performance. Next, to mitigate issues of high simulation cost associated with large area device simulations, we propose a new way to simplify this microcooler geometry into a single manifold channel (SMC) model, which enables up to 10x reduction in simulation expense while simultaneously achieving low simulation error of ± 5%. The SMC model is then validated against numerical simulation of 1/4th scale devices performed by Piazza et al. [16] for varying sizes of the cooler (25–400 mm^2), which later elucidated that the accuracy of this SMC model simulation does not deteriorate with increasing device size. This is an extremely serendipitous finding since full scale, very large 2-level MMC device (> 500 mm^2) simulations which were extremely expensive and cumbersome to perform can now be completed rapidly using this SMC approximation with < 5–7% error in the results. This SMC model is further compared against conventionally used CP only U-bend channel (SCPUC) model [4,14,19–26] to show that the SCPUP model massively underestimates the heat transfer coefficients as compared to the SMC model thus validating the claim made by Boteler et al. [13] and Arie et al. [14] about the thermofluidic coupling between the MF and the CP. Later, detailed flow pattern analysis and comparison of the SMC and the SCPUC revealed that flow redistribution and specific circulation patterns introduced within the CP channels by the manifold, is the major contributing reason for massive differences in prediction between the SMC and SCPUC model. Comparison of the SMC and SCPUC model results simultaneously demonstrated that the conventionally used and popular SCPUC model simulations often produced results with significant error percentage (25–65%) and thus should not be used for making absolute predictions about the thermofluidic performance of 3DMMCs. Finally, to optimize the design, a small parametric study is performed using the SMC and the SCPUC models by varying a few important geometric parameters of the MMC design. The thermofluidic results obtained were analyzed using simple theoretical dimensional estimates to help elucidate how changing different geometric parameters affect the thermal and hydraulic performance of the device. The COPs recorded by the coolers in this study are also reported. When plotted against COPs of existing cooling solutions (jets, single-pass MMC, fins, single-level MMC) it shows the promise of an order of magnitude improvement. One design was recorded to have extremely high COP of 50,144, while the best performing design would be capable of dissipating a record > 1.4 kW/cm^2 all the while maintaining single phase laminar device operation.

1.1. Novel two-level vs conventional single-level MMC

The Manifold in the MMC design in this study has been chosen to be 2-level (Fig. 1(c)) and is similar to ones investigated upon by previously by Piazza et al. [16] and Jung et al. [17,18]. The choice of 2-level 3D manifold instead of the familiar and much easier to fabricate single-level manifolds (Fig. 1(b)), is enabled by recent success in development of cleanroom-based microfabrication techniques for reliably and repeatably making two-level, large area (> 600 mm^2), tall (1 mm) manifolds [15]. Silicon is chosen as the material for the cooler since this will enables direct attachment of the cooler to the chip backside and thus reducing conduction resistances associated with intermediate layers like the lid, TIM etc. Silicon microfabrication also enables us to make micron level channels, which is key for obtaining superior convection performance. The overall cooler design consists of two Silicon wafers – (i) Cold Plate (CP). This is the relatively thin (300–500 μm) layer of the MMC which is responsible for convective heat transfer and sits directly on the heat producing chips in real-application scenarios (Fig. 1(a)). For characterizing the cooler experimentally, photolithographically defined thin (< 500 nm) metal lines are laid on top of the CP, the side that is supposed to be attached / bonded to the hotspot – these metal lines act as resistive heaters, employing Joule heating to provide extreme levels of heat flux and simulate actual hot chips. While simulating the cooler, we have not modelled this thin metal layer but applied heat flux boundary condition at this surface. The other side of the CP has straight channels (also lithographically defined) deeply etched into the wafer. These channels will be the primary site of forced convection-based heat transfer – cooling water flowing through these channels will carry away the heat flux provided by the metal heater on the other side. (ii) Manifold (MF) – The second layer is a comparatively thicker (> 0.5–1 mm) Silicon wafer, which consists of alternating inflow and outflow channels to supply and extract fluid from the CP in a 3D (top-down direction) fashion. The MF is bonded to the CP such that the inflow and outflow channels in the MF are oriented perpendicularly to the channels in the CP. Thus, the CP channels form short fluidic bridge-like connections between a set of adjacently placed manifold inflow and outflow channels (Fig. 1(l),(m)). The length of the bridge (usually ~0.2–0.8 mm) depends on the manifold side channel widths and is much smaller than the heater side length (5–24 mm) – this reduced flow length in the CP channel makes it possible for an MMC configuration to drastically reduce device pressure drop. The MF inflow channels are also connected to two plenums on both sides of the heated zone, the plenum is responsible for distributing cooling fluid coming from the two inlets on both sides, somewhat uniformly among the MF inflow channels. These MF inflow channels then carry the fluid towards the center of the device – during this process, cooling fluid also fills up the CP channel bridges, by making a vertical turn from the manifold into the CP (Fig. 1(l),(m)). After extracting heat in the CP bridges, the now relatively hotter outgoing fluid streamlines encounters the MF outflow channel, which provided path for the fluid to flow out of the device. The arrows (color represents fluid temperature) in Figs. 1 and 2 indicate some representative flow paths in a 3DMMC.

This 2-level 3D manifold (Fig. 1(i)) differs from a single-level manifold (Fig. 1(h)), in only one respect – the orientation and direction of the inflow and outflow ports. Fig. 1 compares the design and streamline paths in detail between 2-level and single-level MMCs. 1-level manifold has inlet on one side of the active area and outlet on the other, while in 2-level manifolds, there are two inflow ports on two sides of the heater and the outflow happens in a top-down 3D fashion from the active area (Fig. 1(d–g)). The top-down fluid extraction (Fig. 1(m)) in a 2-level manifold is enabled by outflow channels that are completely etched through the layer, while the inflow ports which are partially etched are connected to the two inlet ports on either side of the heated area (Fig. 1(i)). The flow path and inflow, outflow channel orientation is shown clearly in Fig. 2 as well. In contrast, single-level MFs have their inflow and outflow channels etched to the same level – all the inflow channels connecting to the inlet port on one side while the alternating outflow channels connect to the outlet port on the other side (Fig. 1(h)). Fabrication of inflow and outflow channels to be at the same depth (like in a 1-level MF) is easy, employing a single-sided etching step to fabricate such manifolds. Fabrication of 2-level manifolds is comparatively difficult, requiring a well characterized double-sided extremely deep Si etching-based process flow [15]. Nevertheless, 2-level manifolds provide the potential to significantly improve device COP over existing single-level manifolded coolers by further shortening the outflow path of the fluid to exit the device.

Firstly, in a 2-level MMC, the total coolant flux is split into two inflowing ports placed on either side of the heater footprint. This means, each of the inlet ports carry half the total device mass flux and serve only half the length of the manifolds.

$$\dot{m}_{total,\ 1-level} = \dot{m}_{per\ inlet,\ 1-level} = 2\dot{m} \tag{1}$$

$$\dot{m}_{total,\ 2-level} = 2\dot{m}_{per\ inlet,\ 2-level} = 2\dot{m} \tag{2}$$

The number of MF channels are still the same between 1-level and 2-level devices, but due to mass flux being halved per inlet in the 2-level MF, the fluid flow velocity and Re in the MF channels are also halved for the 2-level devices.

$$\begin{aligned} n_{MF,1-level} = n_{MF,2-level} &= L/(2W_{MF-wall} + W_{MF-in} + W_{MF-out}) \\ &= L/2(W_{MF-wall} + W_{MF}) \end{aligned} \tag{3}$$

$$\begin{aligned} m_{MF,1-level} &= m_{per\ inlet,1-level}/n_{MF,1-level} = 2\dot{m}/n_{MF,1-level} \\ &= 4\dot{m}(W_{MF-wall} + W_{MF})/L \end{aligned} \tag{4}$$

$$\begin{aligned} m_{MF,2-level} &= m_{per\ inlet,2-level}/n_{MF,2-level} = \dot{m}/n_{MF,2-level} \\ &= 2\dot{m}(W_{MF-wall} + W_{MF})/L \end{aligned} \tag{5}$$

$$\begin{aligned} Re_{MF,1-level} &= \left(\frac{4A_{MF}}{P_{MF}}\right)\frac{4\dot{m}(W_{MF-wall} + W_{MF})}{L}\frac{1}{\mu A_{MF}} \\ &= \frac{8\dot{m}(W_{MF-wall} + W_{MF})}{\mu L(H_{MF} + W_{MF})} \end{aligned} \tag{6}$$

$$\begin{aligned} Re_{MF,2-level} &= \left(\frac{4A_{MF}}{P_{MF}}\right)\frac{2\dot{m}(W_{MF-wall} + W_{MF})}{L}\frac{1}{\mu A_{MF}} \\ &= \frac{4\dot{m}(W_{MF-wall} + W_{MF})}{\mu L(H_{MF} + W_{MF})} = \frac{1}{2}Re_{MF,1-level} \end{aligned} \tag{7}$$

The phenomenon of 50% reduction in Re in MF section by using a 2-level MF indicates that these devices can maintain laminar conditions at larger mass flux levels (up to twice the mass flux value at which a single-level MMC will transitions to turbulence) – a characteristic that eventually leads to well-behaved, easily predictable, and thus controllable performance of MMCs, withal low ΔP.

In addition to mass flux and Re being halved in the MF channels of the 2-level devices, we also notice shortening of coolant liquid flow path within the device. The two inlet ports on two sides of the heater each serves half of the heated area and thus half of the MF. Incoming cold fluid is pushed from two opposite directions through the inflow ports to meet in the device center, thus reducing the maximum fluid flow length within the MF to half of the device length ($L/2$). This reduction in flow path is enabled by the top-down fluid extraction scheme (Fig. 1(g)) where hot fluid after

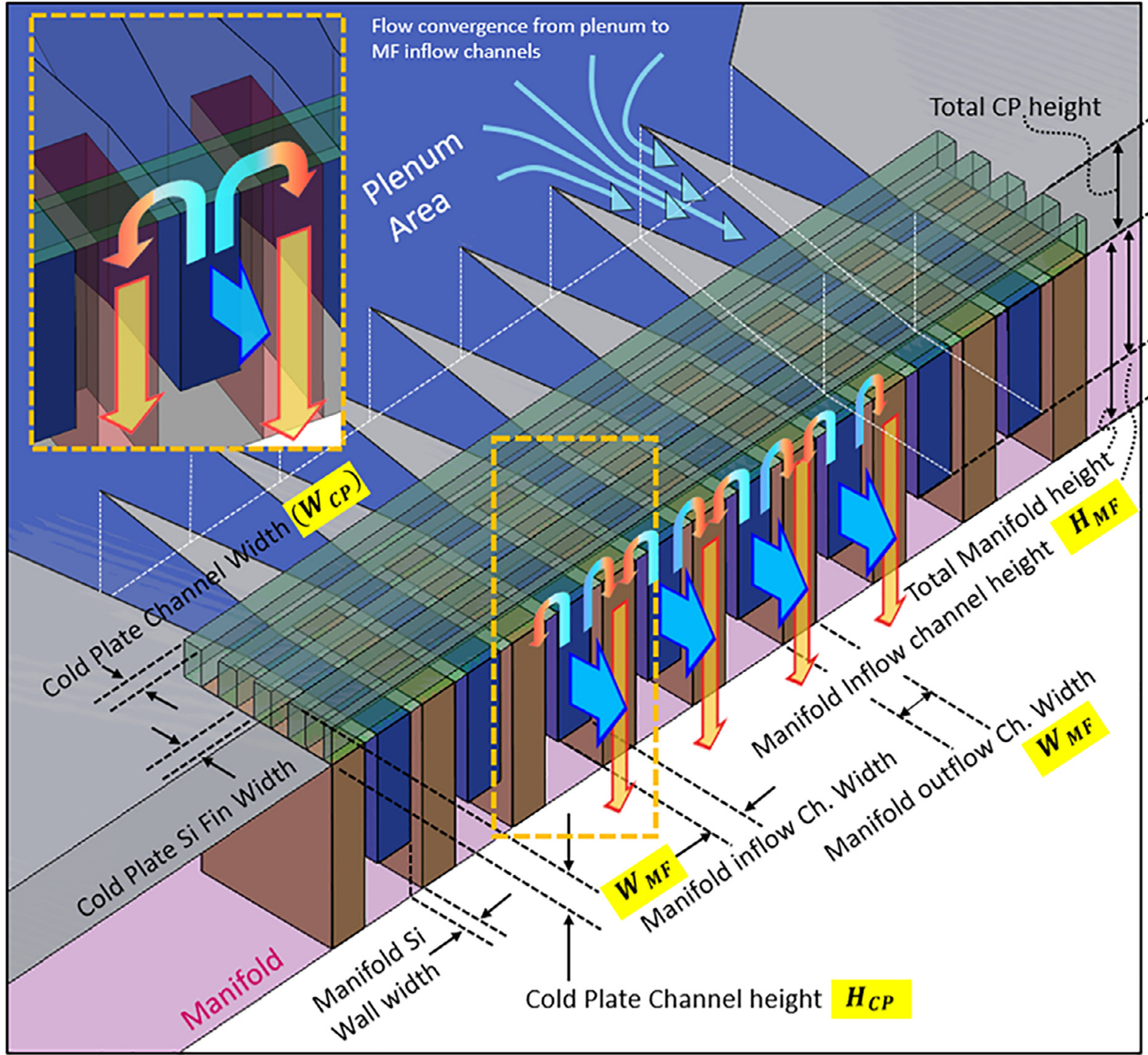

Fig. 2. Cross section of a fully assembled 2-level MMC and fluid flow and heat transfer within it. Blue Section → inflow, Orange section → outflow. All the relevant geometric parameters are also marked – Manifold Channel Width (W_{MF}), Manifold Inflow Height (H_{MF}), CP Channel Width (W_{CP}), CP Channel Height (H_{CP}).

exchanging heat in the CP channel bridges can immediately leave the device via the through etched outflow channels. In contrast, in 1-level MFs, the flow path is always as large as the device length (L) – cooling fluid even after exchanging heat in the CP is forced to travel the entire device length (L) within the manifold channels (from inlet to outlet port) before leaving the device. Based on halved mass flux and halved flow path, a naïve order of magnitude estimate for the Poiseuille pressure drop is possible within the MF.

$$\begin{aligned}\Delta P_{MF,1-level} &\sim \frac{\mu L m_{MF,1-level}}{\rho A_{MF}^2} \\ &\sim \frac{\mu L}{\rho (W_{MF})^2 (H_{MF})^2} \frac{4\dot{m}(W_{MF-wall}+W_{MF})}{L} \\ &\sim \frac{4\dot{m}\mu(W_{MF-wall}+W_{MF})}{\rho (W_{MF})^2 (H_{MF})^2}\end{aligned} \tag{8}$$

$$\begin{aligned}\Delta P_{MF,2-level} &\sim \frac{\mu\left(\frac{L}{2}\right) m_{MF,2-level}}{\rho A_{MF}^2} \\ &\sim \frac{\mu\left(\frac{L}{2}\right)}{\rho (W_{MF})^2 (H_{MF})^2} \frac{2\dot{m}(W_{MF-wall}+W_{MF})}{L} \\ &\sim \frac{\dot{m}\mu(W_{MF-wall}+W_{MF})}{\rho (W_{MF})^2 (H_{MF})^2} \sim \frac{1}{4}\Delta P_{MF,1-level}\end{aligned} \tag{9}$$

The expressions above indicate that the pressure drop in 2-level MFs are at least 4 times lower than 1-level MFs with the same geometry. Next, we will attempt to quantify the average flow conditions within the CP too as induced by the 2-level and 1-level MFs. In 2-level MF devices, even though each inlet in the 2-level MF carries half the total device mass flow rate, they also only feed half the active area each, thus serving half of the total number of CP channels across the entire heated section – this means that the CP channel flow conditions remain unchanged even when we change MF design from 1-level to 2-level. The CP channel mass flux, under the simplified assumption that the MF distributes fluid equally between all the channels, can be written as follows:

$$n_{CP,1-level} = n_{CP,2-level} = L/(W_{CP} + W_{CP-wall}) = L/2W_{CP} \tag{10}$$

$$m_{CP,1-level} = \frac{m_{MF,1-level}}{n_{CP,1-level}} = \frac{8\dot{m}(W_{MF-wall}+W_{MF})W_{CP}}{L^2} \tag{11}$$

$$m_{CP,2-level} = \frac{m_{MF,2-level}}{\frac{1}{2}n_{CP,2-level}} = \frac{8\dot{m}(W_{MF-wall}+W_{MF})W_{CP}}{L^2} = m_{CP,1-level} \tag{12}$$

As shown above, since the mass flux per CP channel stays unchanged between the two MF designs, we can assume that the total thermal performance also stays relatively unchanged. There will, however, be minor variations because of variations in how the two MF designs will distribute the cooling fluid between the CP channels – this has not been captured by the simple theoretical estimates. Same mass flux additionally indicates that the approximate pressure drop within the CP channels will also be equal between the two MF designs chosen. The dependence of CP pressure drop can also be naïvely represented by Poiseuille flow equation as follows:

$$\Delta P_{CP,1-level} \sim \frac{\mu L_{flow-CP\ bridge}\left(m_{CP,1-level}\right)}{\rho A_{CP}^{2}} \sim \frac{\mu\left(W_{MF-wall}+W_{MF}\right)}{\rho\left(W_{CP}\right)^{2}\left(H_{CP}\right)^{2}}\frac{8\dot{m}\left(W_{MF-wall}+W_{MF}\right)W_{CP}}{L^{2}} \sim \frac{8\mu\dot{m}\left(W_{MF-wall}+W_{MF}\right)^{2}}{\rho\left(W_{CP}\right)\left(H_{CP}\right)^{2}L^{2}} \sim \Delta P_{CP,2-level} \tag{13}$$

Based on these theoretical estimates, the COPs of MMC devices (given by the ratio of total heat provided to the hotspot and the total cooling power required to cool this heat load) with 1-level and 2-level MFs can be estimated too.

$$COP_{1-level} = \frac{q'' A_{heater}}{m_{total,1-level}\left(\Delta P_{CP,1-level}+\Delta P_{MF,1-level}\right)} \tag{14}$$

$$COP_{2-level} = \frac{q'' A_{heater}}{m_{total,2-level}\left(\Delta P_{CP,2-level}+\Delta P_{MF,2-level}\right)} = \frac{q'' A_{heater}}{m_{total,1-level}\left(\Delta P_{CP,1-level}+\frac{1}{4}\Delta P_{MF,1-level}\right)} \tag{15}$$

The total pressure drop in these devices are comprised of pressure drop from both the MF and CP side. It has been found that the relative contribution of the MF and CP to total device ΔP depends strongly on the size of the active area. For smaller heater footprint (25 mm^2) the MF side contribution is 30–40% of the total ΔP while for larger devices (400–600 mm^2 heater footprint), the MF side contributes much more, ~65–75%. Based on these percentage contributions, while switching from 1-level to 2-level MFs, COP is theoretically predicted to increase by 30–40% in smaller devices and by 100–150% in larger devices. The increase in COP by switching MF design from 1-level to 2-level, is much more appreciable for large area coolers – this is a strong rationale for adopting 2-level MFs for large area, high performance EMMCs.

1.2. Simulation models, governing equations and boundary conditions

Several studies have attested to the usefulness of simulating 3DMMCs, since the simulated device thermal performance was found to be within experimental error range. The difference between simulation and experimental results are within ± 10% of each other [17,18], this difference was also found to reduce with increased device flow rate. Jung et al. in a subsequent study used numerical simulations of quarter-cut models to perform a parametric optimization of a small area (cooler footprint = 25 mm^2) cooler. They had used ~ 23–24 million mesh elements to resolve microchannels of width 50 μm [17]. These devices were later scaled up by Piazza et al. [16] who used similar simulation methodology to simulate larger coolers of heater footprint sizes of 100 and 400 mm^2. To maintain similar mesh element sizes and resolution near the smallest microchannels, the larger cooler models would require > 70 (100 mm^2 cooler) and > 150 (400 mm^2 cooler) million mesh elements, which are way beyond the capabilities of even powerful workbenches. Thus, to make the simulations more manageable, the mesh sizes were increased and some of the resolution compromised – the simulations were finally performed with > 40 (100 mm^2) and ~65 million (400 mm^2) mesh elements by Piazza et al. with the simulation time of each data point for the large 400 mm^2 devices being 3–4 days. Simulations of larger 25 × 25 mm^2 cooler devices proved impossible using the workstation. Later, an upgraded workstation was used by Wei et al. [29] to accurately model a large 625 mm^2 cooler with total simulation times ranging over 1 week per data point. Additionally, devices with ⟨ 50 μm CP channels and total footprint size ⟩ 250 mm^2 are extremely expensive to simulate using conventional quarter-cut models – this expense prevented mass simulations driven geometrical optimization of the 3DMMC cooler, a crucial step before device fabrication. A clear need was felt to develop a simpler model which can significantly reduce the simulation cost, thereby enable rapid simulations on such 3DMMC devices even if it is accompanied by a decrease in prediction accuracy.

Two candidate reduced order models were considered for the simplification of the full 2-level 3DMMC design. This was possible because the overall MMC can be broken into smaller repeating unit-cells:

(1) Single Cold Plate U-bend Channel Model (SCPUC) – This model considers the flow of coolant only in the U-bend section of the CP channels connecting a set of adjacent manifold inflow and outflow channels. (Fig. 3(e),(f) and (h)) This approach of ignoring the manifold altogether has been very popular, being adopted by several other prior studies [4,14,19–26]. This model assumes that the incoming fluid is first distributed uniformly among the manifold channels, and then again uniformly spread out by the manifold channels among all the CP channel bridges connecting the manifold inflow and outflow channels. Fig. 3(e) shows how the full model has been cut to construct the simplified SCPUC model. This model is extremely appealing to researchers since it is very simple, and simulations usually take a short time (< 0 min per data point) to converge with good convergence behavior. Additionally, the simplicity of the SCPUC model enables us to fully parametrize it using design modeling software. Full parametrization of the geometry enables us to make the overall simulation flow (model making → meshing → Perform simulations with appropriate B.C. → post-processing) fully automatic rather than automated or partially automatic. This way extensive sets of simulations with varying geometry, flow conditions, heat load can be performed automatically without requiring human intervention or monitoring. The ability to simulate hundreds and thousands of simulations automatically allows researchers to perform multi-objective dimension optimization with ease.

(2) Single Manifold Channel model (SMC) – This model is slightly more complicated compared to the SCPUC model and considers the effect of the manifold as well in addition to the CP channels. Each SMC model considers quarter-cut model of one set of MF inflow and outlet channels. Fig. 3(a)–(d) shows how it is obtained by cutting the overall device along the center of adjacent manifold inflow and outflow channels. This model is partly inspired from simplifications made by Arie et al. [14] to their single-level-MMC design, where only one CP channel bridge was considered across one manifold inflow and outflow channel set. Our model differs from Arie's by considering all the CP channels bridges connecting the manifold inflow and outflow, thus also considering non-uniform fluid distribution within the CP induced by the manifold. The non-uniform flow distribution in the CP channels provide us with critical information about the heater temperature map, non-uniformity, hotspot location which are extremely important during the designing phase of an MMC. These models, however, are complex and cannot be fully parametrized easily using 3D modeling software, which

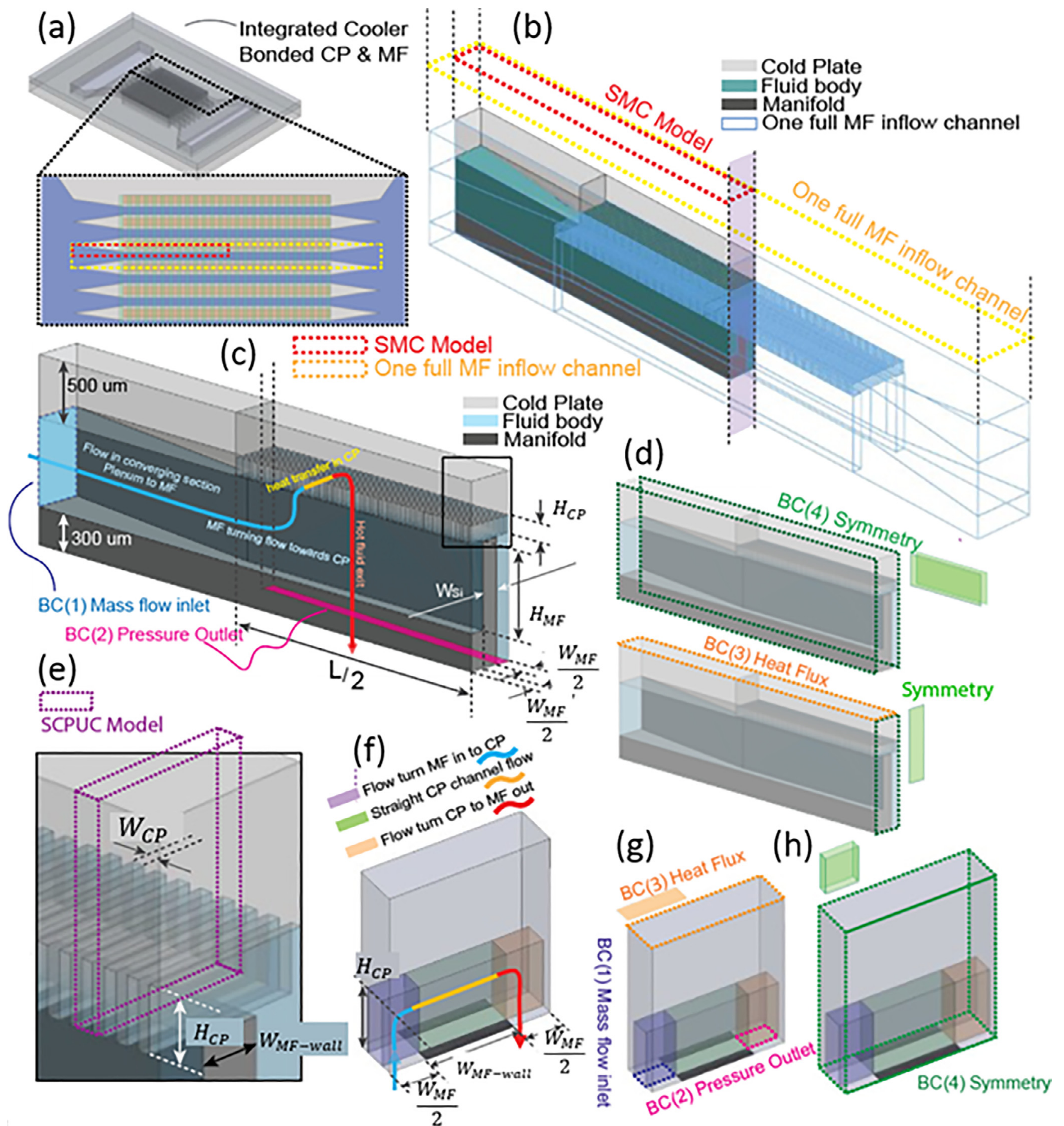

Fig. 3. (a) Integrated cooler isometric view showing CP channels oriented perpendicularly with MF channels. Also shows top view of a few MF channels in a typical 2-level 3DMMC cooler. (b) Isometric view of one set of MF inflow outflow channels forming a unit cell that can repeat to make up the entire cooler. Yellow rectangle indicates one full inlet/outlet channel set, red rectangle indicates 1/4th of a single set of inflow/outflow MF channels, (c) Isometric view of the SMC model - 1/4th MF channel formed by the red rectangles in (b). Also shows the "mass inflow" and "pressure outlet" face of the model. Additionally, one fluid streamline path is marked (color represents fluid temperature) along with several dimensions. (d) Shows the faces where "symmetry" conditions are applied. (e) Shows how the Single CP U-bend Channel (SCPUC) model has been obtained from the SMC model, (f) Schematic showing fluid flow path within the CP and pertinent geometries, (g,h) SCPUC simulation boundary conditions shown.

robs us of the ability to perform simulations fully automatically. Without fully automatic simulations, extensive design optimization using multi-objective optimization was not possible. Although, later in this report, we observe that SCPUC models are highly inaccurate in predicting device performance. Thus, a slightly more complex SMC model, is a small inconvenience to bear for superior prediction accuracy.

Both these models were constructed in a 3D modeling software, Solidworks the fluid domain being water and the solid domain, silicon. "Mesh Dependence Study" was performed on a design to establish a consistent meshing methodology, "E" that was then used to mesh the different designs. More details can be found in the Supplementary Information. Following meshing, conjugate heat transfer simulations were performed under steady, single-phase,

Table 1
Design details of D4 – the design simulated by Piazza et al. [16]. The simulation results of D4 was used to validate SMC model simulation results.

	L	H_{MF}	$MF_{thickness}$	W_{MF-in}	W_{MF-out}	$W_{MF-wall}$	H_{CP}	$W_{CP-wall}$	W_{CP}	$CP_{thickness}$
	mm	µm	µm	µm	µm	µm	µm	µm	µm	µm
D4	51020	750	1000	215	217	200	75	50	50	200

laminar, incompressible flow conditions in a commercial CFD package, ANSYS Fluent. Continuity and momentum equation was solved for the fluid domain while energy equation was considered for both the solid Si and liquid water domains. These equations are listed as follows:

Continuity (fluid domain)

$$\frac{\partial}{\partial x_i}(\rho u_i) = 0 \tag{16}$$

Momentum (fluid domain)

$$\frac{\partial}{\partial x_i}(\rho u_i u_j) = -\frac{\partial P}{\partial x_j} + \frac{\partial}{\partial x_i}\left(\mu \frac{\partial u_j}{\partial x_i}\right) \tag{17}$$

Energy (fluid domain)

$$\frac{\partial}{\partial x_i}(\rho u_i C_p T_{liq}) = \frac{\partial}{\partial x_i}\left(k_{liq} \frac{\partial T_{liq}}{\partial x_i}\right) \tag{18}$$

Energy (solid domain)

$$\frac{\partial}{\partial x_i}\left(k_{sol} \frac{\partial T_{sol}}{\partial x_i}\right) = 0 \tag{19}$$

ANSYS Fluent also enables us to couple the fluid and solid domains for our conjugate heat transfer analysis, by imposing the following flow and energy conditions at the fluid-solid interfaces:

No penetration, no slip:

$$u_n = 0,\ u_t = 0 \tag{20}$$

where u_n and u_t are normal and tangential velocities with respect to the interface where it was set.

Continuity of temperature:

$$T_{sol-int} = T_{liq-int} \tag{21}$$

Continuity of heat flux:

$$k_{sol} \frac{\partial T_{sol}}{\partial x_n} = k_{liq} \frac{\partial T_{liq}}{\partial x_n} \tag{22}$$

where x_n is the normal vector to the interface where conditions are applied.

The user-imposed boundary conditions are specified as follows –

Heat flux of 800 W/cm^2 was specified at the heater surface, while all other solid walls are kept adiabatic.

Heater Surface:

$$q'' = 800 \frac{W}{cm^2} \tag{23}$$

All other Solid Walls:

$$\frac{\partial T_{sol}}{\partial x_i} = 0 \tag{24}$$

The mass flow rate is specified at the inlets of the design. The total device level mass flow rate, $\dot{m}_{total}$ has been kept constant at 0.2 lpm. The $\dot{m}_{total}$ value was chosen to be the same as used by previous studies by Jung et al. and Piazza et al. and thus enables us to compare our results directly with them. However, it is important to note that unlike previous studies which simulated full geometries, we are simulating either 1/4th of one set of MF channels (SMC model) or one CP channel (SCPUC model) and thus the simulated mass flux that is inputted to ANSYS Fluent must be calculated from $\dot{m}_{total}$ by assuming that this flux is being distributed equally among the MF and CP channels. These calculations are performed in the previous section and listed in Eqs. (5) and (12).

Mass flux at inlet (SMC):

$$\dot{m}_{Fluent} = \frac{1}{4}\dot{m}_{MF} = \frac{\dot{m}(W_{MF-wall} + W_{MF})}{2L} \tag{25}$$

Mass flux at inlet (SCPUC):

$$\dot{m}_{Fluent} = \dot{m}_{CP} = \frac{8\dot{m}(W_{MF-wall} + W_{MF})W_{CP}}{L^2} \tag{26}$$

The temperature of the inflowing water was set constant across all designs at 300 K. The outlet was set as "pressure-outlet" indicating gage pressure to be 0 at these locations.

Outlet:

$$P_{gauge} = 0 \tag{27}$$

Finally, the parallel faces that were used to cut the unit-cell (SMC or SCPUC) out of the full device must be set as "periodic" faces indicating that periodicity along those faces would help us construct the full cooler geometry. However, parallelly oriented "periodic" faces without any fluid inflow and outflow on these faces can be simplified into "symmetry" conditions –

Symmetry BC at along unit cell cut-faces:

$$\frac{\partial u_j}{\partial x_n} = 0, \quad \frac{\partial T}{\partial x_n} = 0 \tag{28}$$

where x_n indicates direction vector normal to the faces where the condition has been set.

1.3. Validation of SMC model

The SMC model is first validated by performing simulations using a specific 2-level 3DMMC design (D4 in Jung et al. [17,18] and Piazza et al. [16]) and comparing the results against simulations performed by Piazza et al. [16] First, 3 SMC models were constructed using geometric details of the design "D4" [16–18] with varying footprint size from 25, through 100–400 mm^2. The details of geometry, "D4" has been listed in Table 1.

Following this, the models were meshed according to an optimal Meshing methodology "E" (See Supplementary Information (SI) for "Mesh Dependence Study"). Finally, simulations were performed on each design in ANSYS Fluent v19.0 following the settings and parameters outlined in Table A1 in SI, with heat flux of 800 W/cm^2 and a range of total device flow rates. Power law fits ($Nu \propto Re^x$) are commonly employed by researchers to empirically quantify the thermal performance of coolers as a function of device flow rate and was used to fit the data points obtained through our SMC model simulations. The average chip temperatures and total device ΔPs are plotted and compared for the quarter model simulations performed by Piazza et al. and SMC model simulations for three different device sizes (Fig. 3). The percentage differences between predictions in average chip temperature and device ΔP of these two models are displayed as vertical columns on the same plot.

Table 2
All 54 designs simulated using SMC model by varying H_{MF}, W_{MF}, H_{CP} and W_{CP}. Constants are as follows – $\dot{m}_{total} = 0.2\ lpm$, $q'' = 800\ W/cm^2$, $CP_{thickness} = 500\ \mu$m and $W_{MF-wall} = 150\ \mu$m. There are two constraints imposed, $W_{CP} = W_{CP-wall}$ and $W_{MF} = W_{MF-wall}$.

Design #	H_{MF}	W_{MF}	H_{CP}	W_{CP}	Design #	H_{MF}	W_{MF}	H_{CP}	W_{CP}
	μm	μm	μm	μm	–	μm	μm	μm	μm
1	700	100	75	15	**28**	1500	100	75	15
2	700	100	75	50	**29**	1500	100	75	50
3	700	100	75	90	**30**	1500	100	75	90
4	700	100	225	15	**31**	1500	100	225	15
5	700	100	225	50	**32**	1500	100	225	50
6	700	100	225	90	**33**	1500	100	225	90
7	700	100	375	15	**34**	1500	100	375	15
8	700	100	375	50	**35**	1500	100	375	50
9	700	100	375	90	**36**	1500	100	375	90
10	700	250	75	15	**37**	1500	250	75	15
11	700	250	75	50	**38**	1500	250	75	50
12	700	250	75	90	**39**	1500	250	75	90
13	700	250	225	15	**40**	1500	250	225	15
14	700	250	225	50	**41**	1500	250	225	50
15	700	250	225	90	**42**	1500	250	225	90
16	700	250	375	15	**43**	1500	250	375	15
17	700	250	375	50	**44**	1500	250	375	50
18	700	250	375	90	**45**	1500	250	375	90
19	700	450	75	15	**46**	1500	450	75	15
20	700	450	75	50	**47**	1500	450	75	50
21	700	450	75	90	**48**	1500	450	75	90
22	700	450	225	15	**49**	1500	450	225	15
23	700	450	225	50	**50**	1500	450	225	50
24	700	450	225	90	**51**	1500	450	225	90
25	700	450	375	15	**52**	1500	450	375	15
26	700	450	375	50	**53**	1500	450	375	50
27	700	450	375	90	**54**	1500	450	375	90

1.4. Parametric analysis

Validation of the SMC model's accurate thermofluidic prediction capability along with fast simulation time (∼1–3 h as compared to ∼ 24–48 h for quarter device simulation) allows the possibility of performing extensive simulation driven design optimization. This is an important step before fabrication of actual coolers which is expensive and time-consuming. Furthermore, the wealth of simulation data generated through design will act as a glossary of MMC designs to serve as a design guide for targeted applications. This information will also be used in future studies to validate theoretical models.

Since SMC model simulations are semiautomatic and requires manual intervention from time to time, extensive database generation (∼1000 simulation data points) is difficult. Therefore, a smaller design experiment was formulated by considering variations in the relevant important geometries of the MMC. The main parameters that determine the device performance were found to be the CP side channel dimensions which directly affects the hydraulic diameter and thus thermal performance of the cooler. CP channel width (W_{CP}) were chosen to be 15, 50, and 90 μm to cover a wide range of channel widths possible through different manufacturing techniques. The solid silicon wall width ($W_{CP-wall}$) between the CP channels is also an important parameter, which determines the fin efficiency of the CP, the amount of conduction-coupling that exists between the CP fluid bridges and the number of CP channels in the overall active area. For our cases, $W_{CP-wall}$ is always kept equal to W_{CP} such that CP channel fraction is 0.5 for all designs with respect to the total active cooling area, L^2. CP height (H_{CP}) values were selected to be 75, 225 and 375 μm – this covers a wide range of CP channel heights. The total solid CP thickness is kept constant at 500 μm to comply with actual fabrication scenarios where the CP channels will be etched into a 500 μm thick Si wafer. The thickness of this solid Si, H_{Si} between the fluid channels and the hotspot, is related to H_{CP} as, $(H_{Si} = CP_{thickness} - H_{CP})\ \mu m$.

The Manifold side channel dimensions primarily affect the fluid distribution and thus the hydraulic performance of the device. For simplicity, inflow (W_{MF-in}) and outflow (W_{MF-out}) channel widths were set equal and abbreviated W_{MF} throughout the rest of this letter. Its values were also chosen to maximize range, 100, 250 and 450 μm. The Silicon wall width ($W_{MF-wall}$) separating the inflow and outflow channels need to be as small as possible to maximize the area available for liquid delivery and extraction. This was set constant across all designs to an arbitrary low value of 150 µm – further reduction will improve thermofluidic performance but compromise mechanical strength and robustness of the device during fabrication and testing. The final MF parameter, inflow channel heights (H_{MF}) were chosen, 0.7 and 1.5 mm. The total hotspot size (active cooling area) is 5 × 5 mm^2 (device length = 5 mm), for the initial design study – this ensures that for all the designs considered, the flow within is always laminar thus reducing simulation complexity even further. For each design and their input mass flow rates, the *Re* has been calculated in different sections and they were all verified to be < 1500, thus confirming fully laminar device operation. This study is also currently being extended to larger device sizes (25 × 25 mm^2), although for larger devices, flow conditions would lead to both laminar and turbulent regimes which will need to be accounted for carefully during simulation setup. The design of experiment finally yielded 54 total geometries. The geometric details have been listed in Table 2. We will follow a nomenclature scheme, $W_{MF} - H_{MF} - W_{CP} - H_{CP}$ to identify and refer to each of these designs throughout the rest of this letter.

The next step is to simulate these device designs under the same heating load or flux ($q'' = 800\ W/cm^2$) and total device-level inflowing coolant water flow rate ($m_{total} = 0.2\ lpm$) to compare their performances. We reiterate that the total device flow rate, m_{total} has been kept constant, 0.2 lpm across the geometries and since we have simulated only one MF channel (SMC model) and only one CP channel (SCPUC model), we appropriately adjusted the m_{total} into m_{MF} and m_{CP} for every design separately before in-

putting mass flux in the Fluent models. For the SMC models, $\dot{m}_{MF}$ was calculated by dividing $\dot{m}_{total}$ by the number of MF channels, n_{MF} and then again by 4 (SMC model is one quarter of a full set of MF channels) it was assumed that the total inflowing flux m_{total} is distributed by the plenum equally among the different MF channels. This assumption has been tested to hold true by Wei et al. [29] who simulated quarter-device model for a large area 3DMMC device and plotted MF channel velocities near the edge and center of the device. For the SCPUC simulations, $\dot{m}_{CP}$ was further calculated by dividing $\dot{m}_{MF}$ by the number of CP channels, n_{CP} by additionally assuming that each MF channel distributed fluid equally among the CP channels – however, this assumption is invalid and leads to erroneous junction temperature maps as predicted by the SCPUC simulations.

The SMC designs were meshed in accordance with methodology "E", which was found to be the optimal methodology after performing "Mesh Independence Study" (more details in Supplementary Information). The CP channels are the thinnest sections of the device and the site for convective heat transfer; thus they must be resolved accurately during meshing. 15 μm wide CP channels were meshed using 5 hexahedral cut-cells (~3 μm size), 50 μm channels via 10 cells (~5 μm cell size) and 90 μm channels using 15 (~6 μm size) cells.

The SCPUC simulations of the 54 designs were much simpler since the geometry consists of only a U-bend straight channel which do not require extensive mesh dependence study. The mesh for these can be easily refined to sub-micron levels using "growth rate" of 1.01 and "Number of Cells Across gap" value of $>$ 20 (resulting in $<$ 1 μm elements). Number of mesh elements were recorded to be $>$ 50,000 in all cases. These simulations were performed overnight using an ANSYS Fluent automation script, since their designing step can be fully parametrized, and simulation process can be made completely automatic.

The simulations were then investigated upon with the aid of some naïvely developed theoretical estimates, to ascertain the effect of changing different geometrical parameters of the SMC model on thermal and fluidic performance. The difference in prediction between the SMC and SCPUC were also examined closely. In addition to plotting relevant parameters, extensive flow pattern, contour and streamline analyses were performed both on the SMC and the SCPUC model to understand the flow behavior within such 3DMMC devices.

2. Results and discussions

2.1. SMC model validation

Fig. 4(a–f) plots percent difference in thermal and hydraulic performance prediction (average chip temperature) between the SMC model and detailed quarter-cut device simulations as performed by Piazza et al. for design "D4" [16]. SMC prediction of total ΔP (Fig. 4d–f) shows high percent difference as compared to quarter-cut model, which worsens at higher flow rate values. Maximum difference increased from 8% (25 mm^2) through 15% (100 mm^2) to 20% (400 mm^2) as device size was increased. This is expected since, the SMC model neglects large portions of the flow in the inlets, plenums and thus underpredicts the total device ΔP – the effect becomes more pronounced for higher flow rates in large devices. Interestingly, even though the SMC model shows large differences in ΔP prediction at higher flow rates, it is still able to accurately capture the thermal performance (chip average temperature) often with better accuracy with increasing device size. This can be observed in Fig. 4(a–c), where the percent error in the SMC model thermal predictions do not increase beyond 5% even with increase in total device size. This finding is extremely fortuitous, since it indicates that this SMC model simplification can be successfully implemented without any loss of prediction accuracy for large area coolers ($>$ 400 mm^2) which otherwise are not possible to simulate. This observation, however non-intuitive at first, can be explained by noting that, with the increase in total chip size, the number of manifold channels, n_{MF} given by Eq. (3) also increases (from 6 in 25 mm^2 to 12 in 100 mm^2 and 24 in 400 mm^2). Increasing device n_{MF} takes it geometrically closer to the SMC model approximation, which assumes an infinitely repeating array of alternating MF inflow and outflow channels – thus SMC model predictions still perform well and can maintain low prediction error even with increasing device size and complexity.

It is worthwhile to note that device scale up is also inherently associated with a change in flow physics within the device leading to earlier transition to turbulence. This is the result of the 3D manifolded device configuration. While scaling up a device from a smaller area, $A_1 = L_1^2$ to a larger $A_2 = L_2^2$, equivalent mass flow rates scale with the device area (L^2) according to the cooler energy balance equation:

$$q'' A_h = \dot{m}_{total} C_p \ \Delta T_{sens}, \ \dot{m}_{2-equiv} = \dot{m}_{1-equiv}\left(\frac{L_2}{L_1}\right)^2 \tag{29}$$

However, the number of MF and CP channels, n_{MF} and n_{CP} scale with the device side-length, L, according to Eqs. (3) and (10). Thus, for isoheating and cooling cases, dependence of equivalent mass flow rates and Re in each MF and CP channels can also be written as:

$$Re_{MF} \ \sim \ m_{MF} = \dot{m}_{total}/n_{MF} \ \sim \ L^2/L \sim \ L \tag{30}$$

$$Re_{CP} \ \sim \ m_{CP} = \dot{m}_{total}/(n_{MF})(n_{CP}) \ \sim \ L^2/(L)(L) \ \sim \ 1 \tag{31}$$

These expressions show that on increasing device size but keeping the heating load and equivalent mass flux constant, the averaged CP flow conditions remain unchanged, however the Re in MF increases (scaling linearly with the device size, L). This explains why while scaling from smaller to larger devices, we observe turbulence within the MF for mass flux much lower than the scaled equivalent mass flux as seen in Fig. 4. This effect should be carefully considered while performing simulations.

Furthermore, we observe that the SMC model overpredicts average chip temperature for the smallest (25 mm^2) device, but underpredicts it for the larger (100 and 400 mm^2) devices. This is observed since the SMC approximation completely ignores the conduction heat loss by the solid Silicon around the hot-spot, that the cooler is made of. In the quarter model simulations, this conduction heat loss affects the overall chip temperature by bringing down the temperature of a small peripheral zone around the hot spot. The width of this zone is often termed "characteristic length" (L_c), and its order of magnitude. It is characterized by the ratio of convection to conduction resistance, kA_c/hP_m like in a fin problem. Relative conduction losses are higher in smaller hotspot (25 mm^2) cases since the characteristic length is significant compared to the device footprint length ($L_c \sim L$). This indicates that a large proportion of total heated area has had its temperature lowered by the conduction loss from the sides. The SMC model simulations fail to capture this temperature lowering effect by the surrounding silicon and thus overpredicts the chip average temperature of the small 25 mm^2 device. In the larger devices, however, the relative importance of the conduction loss to convective cooling is much lower since in the larger devices, the ratio of characteristic length and device size is negligible ($L_c \ll L$) indicating that a very small proportion of the total heated zone has their temperature lowered by the conduction loss from the periphery. In these large devices, the flow maldistribution within the different MF and CP channels plays a more significant role in worsening the thermal performance. The SMC model assumes perfect distribution of fluid

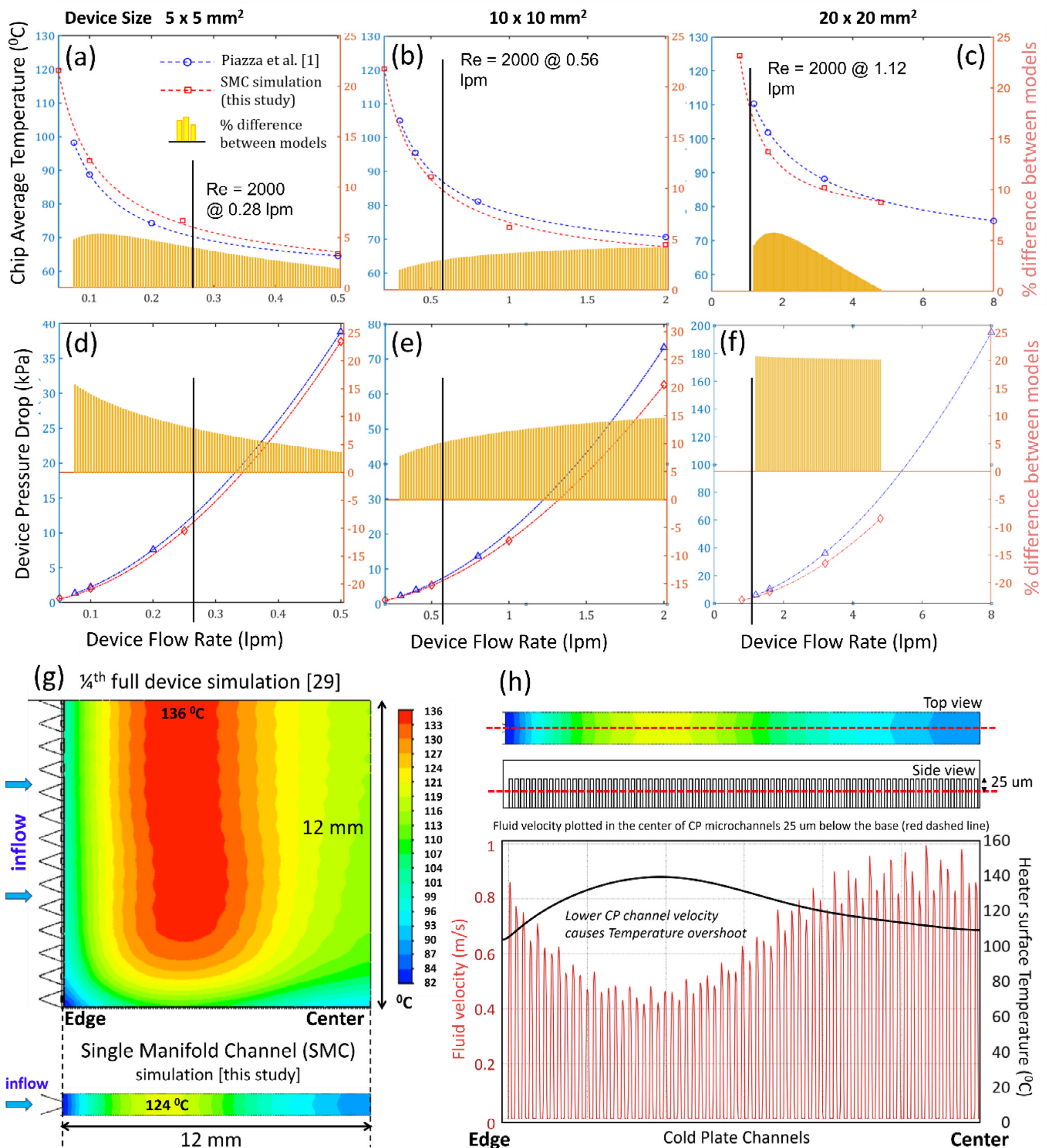

Fig. 4. (a–f) SMC model (red) validated against previous ¼th (quarter device) simulations performed by Piazza et al. [16], on varying sizes of the device – 25, 100, 400 mm^2. (a–c) The thermal performance predictions were limited to 5% irrespective of the device size, which implies that even with increased size of total device footprint, the prediction error by the SMC model does not deteriorate. This is very fortunate, since the results of the quarter model simulations on 600 mm^2 devices which prove to be almost too expensive and cumbersome, can be reproduced with $<$ 5% error using the SMC model. (d–f) There is however a significant error in prediction of total ΔP, which worsens for larger devices and larger flow rates. The error was limited to 15% underprediction in the 25 and 100 mm^2 devices, but 20% in the large 400 mm^2 device – these underpredictions are expected since the SMC model is a significant simplification of the total geometry of the cooler. These plots simultaneously indicate (vertical black line) the flow rates where transition into turbulence occurs for these devices – please note that this transition flow rate is much earlier than equivalent flow rates for the larger devices. This causes higher ΔP in the large devices but simultaneously maintains good cooling performance. (g) Compares the temperature map as predicted by the quarter and SMC model simulation. SMC model underpredicts the maximum temperature by about 7%, but captures the maximum temperature shifting behavior from the device center towards the edge, very accurately.

between all the manifold inflow channels and underpredicts the chip average temperature in these cases – this simultaneously indicates that maximum convective thermal performance can be obtained from a 3DMMC if the plenum is designed to distribute the inflowing fluid as uniformly as possible between the manifold inflow channels. The ΔP predictions by the SMC model, however, are observed to always be much lower than the quarter model prediction by Piazza et al. [16] This can be attributed to the fact that the SMC model neglects the inflow, outflow, plenum sections of the overall device – these sections of the device contribute increasingly to the overall device ΔP as flow rate increases or if the flow behavior changes to turbulent (both of these effects can be observed in Fig. 4).

The temperature maps have also been plotted for a large (24×24 mm^2) device obtained using the quarter and the SMC model simulations in Fig. 4(g). Since device area is large, the SMC model underpredicts the maximum chip temperature by 7%, and average chip temperature by 5%. Furthermore, a surprising phenomenon that was observed by Piazza et al. [16] and Wei et al. [29] was the shifting of the hot-spot maximum temperature location from the device center to the sides with increasing coolant flow rates – this shifting was also observed for our SMC model simulation. Piazza et al. postulated a reason for this observation – that at large flow rates, fluid velocity entering the Manifold channels is very high. The high inertia of the flow pushes the bulk of the fluid predominantly along the manifold channels at the entrance region, thus bypassing the first set of CP microchannels near the entrance. This has confirmed definitively in this study, in Fig. 4(h), where the CP channel velocities are plotted from the edge to the center of the device. We see a drop in fluid velocity in the first set of CP channels close to the edge, which is simultaneously accompanied by a local rise in temperature. The fluid velocity rises again near the center of the device as the rest of the fluid encounters the symmetry boundary condition at the center and is forced to flow up through the CP channels.

2.2. Effect of variation of geometry on 3DMMC thermofluidic performance

Before proceeding with analysis of results, a simple attempt was made to gage the dependence of the total device thermal resistance and its several components on MMC dimensions. Total device thermal resistance is comprised on the convection resistance (R_{conv}) in the CP microchannels, advection resistance (R_{adv}) associated with sensible heat rise of the inflowing cooling water and conduction resistance (R_{cond}) from the solid silicon between the fluid CP channels and the heated surface –

$$R_{total} = R_{conv} + R_{adv} + R_{cond} \tag{32}$$

The simulated values of these components can be written in terms of temperatures at different locations of the SMC model as follows –

$$\frac{T_{chip-avg} - T_{water-in}}{q''A_h} = \frac{T_{CP\ microchannel\ roof} - T_{water-avg}}{q''A_h} + \frac{T_{water-avg} - T_{water-in}}{q''A_h} + \frac{T_{chip-avg} - T_{CP\ microchannel\ roof}}{q''A_h} \tag{33}$$

Here $T_{CP\ microchannel\ roof}$ is the temperature of the roof of the CP channels, $T_{chip-avg}$ captures average temperature of the heated surface. $T_{water-avg}$ is the averaged temperature of the coolant and is calculated by accounting for the sensible heat rise, ΔT_{sens} $(= T_{water-out} - T_{water-in})$ of the inflowing cooling water after exchanging heat at the CP as, $T_{water,avg} = T_{water-in} + (1/2)\Delta T_{sens}$.

Cancelling A_h from all sides enables us to write the Area normalized resistances, $R'' = R \times A_h$.

$$R''_{conv-simul} = \left(T_{CP\ microchannel\ roof} - T_{water,avg}\right)/q'' \tag{34}$$

$$R''_{adv-simul} = \left(T_{water,avg} - T_{water,inflow}\right)/q'' \tag{35}$$

$$R''_{cond-simul} = \frac{\left(T_{chip-avg} - T_{CP\ microchannel\ roof}\right)}{q''} \tag{36}$$

The above-mentioned expressions help us estimate these components directly from simulation results. These are plotted in Fig. 5.

We have also attempted to quantify the dependence of these components on varying geometry. We start with the convection resistance, R_{conv}. A power law dependence assumption that is very commonly used by several researchers to characterize convection dominated problems, was used within the CP, $Nu \sim Re^x$, where x is usually a positive number ≤ 1, and is obtained for each case via best fit to experimental Nu - Re plots. This simultaneously yields a dependence between CP fluid-solid area averaged heat transfer coefficient, h to the average Re within the CP, Re_{CP} as:

$$\begin{aligned}\frac{1}{R''_{conv-theory}} &\sim h \sim (Re_{CP})^x \frac{k}{L_{flow-CP\ bridge}} \\ &\sim \left(\frac{m_{CP}}{\mu A_{CP}} D_{h,CP}\right)^x \left(\frac{k}{W_{MF-wall} + W_{MF}}\right) \\ &\sim \left(\frac{\dot{m} W_{CP}(W_{MF-wall} + W_{MF})}{\mu L^2 (W_{CP} + H_{CP})}\right)^x \left(\frac{k}{W_{MF-wall} + W_{MF}}\right) \\ &\sim \left(\frac{\dot{m}}{\mu L^2 (1+\alpha)}\right)^x \frac{k}{(W_{MF-wall} + W_{MF})^{1-x}}\end{aligned} \tag{37}$$

Where $R''_{conv-theory}$ is the area normalized convection resistance in each CP channel and $L_{flow-CP\ bridge}$ is the length of the CP channel bridges formed by connecting adjacent MF inflow and outflow channels. Note that for analyzing components of thermal resistances, only dimensional dependences are considered, and all numerical coefficients have been dropped. The total thermal resistance associated with convection, $R_{conv-theory}$ is thus related to MMC dimensions as follows:

$$\begin{aligned}R_{conv-theory} &\sim \frac{R''_{conv-thoery}}{A_{CP\ channels}} \sim \frac{1}{hA_{CP\ channels}} \\ &\sim \frac{\left(\frac{\mu L^2 (W_{CP}+H_{CP})}{\dot{m} W_{CP}}\right)^x \frac{(W_{MF-wall}+W_{MF})^{1-x}}{k}}{\left(\frac{L^2 H_{CP}}{W_{CP}} + \frac{L^2}{2}\right)} \\ &\sim \frac{\left(\frac{\mu}{\dot{m}}(1+\alpha)\right)^x (W_{MF-wall} + W_{MF})^{1-x}}{kL^{2(1-x)}(\alpha + 1/2)}\end{aligned} \tag{38}$$

Where α is the CP channel aspect ratio, $\alpha = \frac{H_{CP}}{W_{CP}}$. Even though this theoretical derived dependence relationship is extremely simple and cannot be used for prediction of thermal performance, it will still enable us to interpret the variations in thermal performance (chip temperature) with changing geometrical parameters.

Note that area normalizations for $R_{conv-simul}$ and $R_{conv-thory}$ are different. $R_{conv-theory}$ normalization is done with area, $A_{CP\ channels} = L^2(\alpha + \frac{1}{2})$, since it attempts to capture the heat transfer coefficient averaged over the entire solid fluid contact area in the CP. While $R_{conv-simul}$ normalization was done with the total heater area, $A_h = L^2$, which emerges from the heat flux, q'' defined over the entire heater area, A_h as seen in the definition Eq. (34).

To understand how $R_{conv-theory}$ varies with α, we first differentiate it and obtain the following expression after simplification –

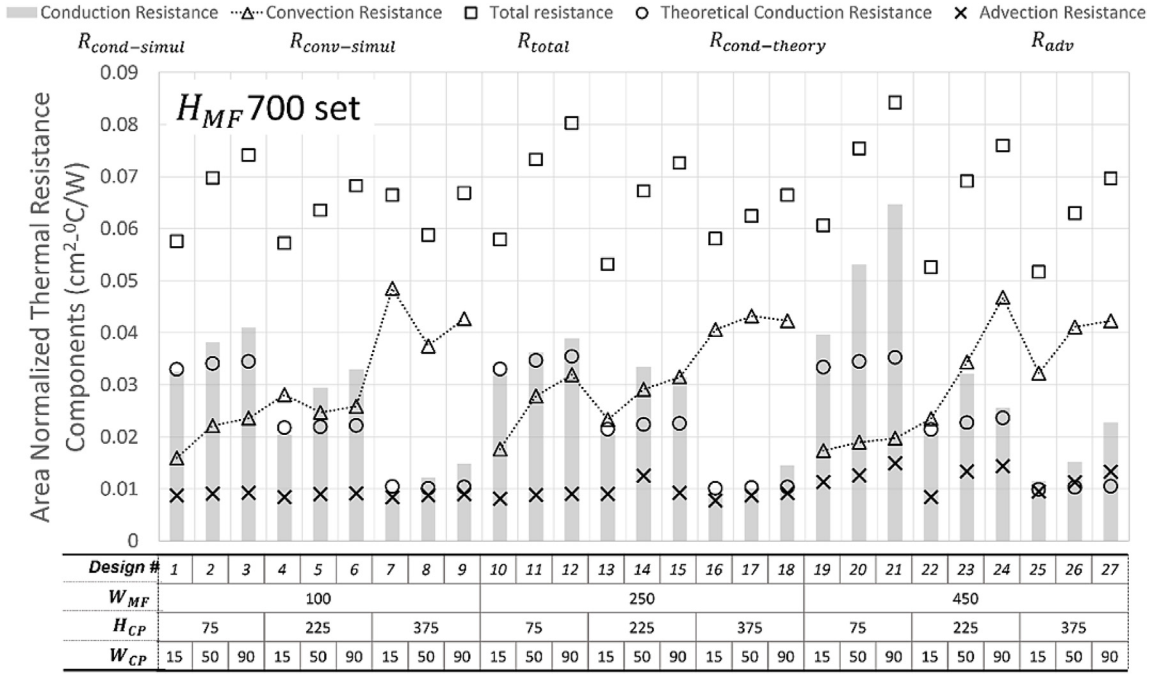

Fig. 5. Plot showing different resistance components of the MMCs. $R_{convection}$ (connected via dotted lines for easy visibility) follows the expected trend of increasing with hydraulic diameter, D_h since increasing D_h is characterized by lower heat transfer coefficient. The change in D_h is also more prominent with H_{CP} and thus $R_{convection}$ is seen to generally increase with H_{CP}. Increasing W_{CP} also contributes to increasing D_h, but to a much smaller degree since $W_{CP} \ll H_{CP}$, thus the contribution on $R_{convection}$ is also nominal.

$$\frac{\partial R_{conv-theory}}{\partial \alpha} \sim \left(\frac{(1+\alpha)^x}{\alpha+\frac{1}{2}}\right)\left(\frac{x\left(\alpha+\frac{1}{2}\right)-(1+\alpha)}{(1+\alpha)\left(\alpha+\frac{1}{2}\right)}\right) \tag{39}$$

We observe that the derivative term is always negative, since $x(\alpha+\frac{1}{2}) < (1+\alpha)$ holds true for all $x \leq 1$. Thus, with increasing α, we observe reduction in $R_{conv-theory}$.

Furthermore, this sensible temperature rise of the inflowing water, ΔT_{sens} enables us to calculate another component of device resistance, termed advection resistance, R_{adv}. For all our designs, the full device level heat load (W) and mass flux has been kept the same, thus leading to the same value of ΔT_{sens} for all designs. This can be seen clearly in the cooler level energy balance shows how ΔT_{sens} is the same across all designs – $q'' A_{heater} = \dot{m}_{total} C_p \Delta T_{sens}$. Consequently, R_{adv} for all designs are also the same.

$$R''_{adv-theory} = L^2/\dot{m}_{total} C_p = 0.018\ cm^2 - K/W \tag{40}$$

Theoretically calculated $R''_{adv-theory}$ was very close to the simulated values of 0.01–0.015 cm^2-K/W as seen in Fig. 5. The final resistance component comes from solid silicon width that exists between the fluidic CP channels and the hotspot. The conduction resistance, R_{cond} in area normalized form can be given as:

$$R''_{cond-theory} \sim \frac{(CP_{thickness} - H_{CP})}{k} \tag{41}$$

Ideally, in the expressions for $R''_{cond-simul}$ and $R''_{conv-simul}$, we would like to have used the average temperature across the entire area of fluid solid contact ($A_{CP\ channels}$), given by $T_{CP\ microchannel\ total}$ in place of the roof only as captured by $T_{CP\ microchannel\ roof}$ but this proved difficult while post processing. The expressions in Eqs. (37) and (38) for $R_{conv-theory}$ however, provides the heat transfer coefficient averaged over the total CP fluid solid contact area. It would thus be related to the average temperature of the total CP area, $T_{CP\ microchannel\ total}$ as:

$$R''_{conv-theory} \sim \frac{T_{CP\ microchannel\ total} - T_{water-avg}}{q''} \tag{42}$$

While $R_{conv-simul}$ only captures heat transfer coefficient locally, based on the temperature of the roof of the microchannels, $T_{CP\ microchannel\ roof}$ (given in Eq. (34)). $T_{CP\ microchannel\ roof}$ is always larger than $T_{CP\ microchannel\ total}$ since the roof is closest to the hotspot and thus, the hottest part of the channels, so $R_{conv-simul}$ as plotted in Fig. 5 will always be an overestimation of the actual R_{conv} in the devices, and will be higher than the prediction by $R_{conv-theory}$. This can be observed in the variation of $R''_{conv-simul}$ with W_{CP} and H_{CP}.

In Fig. 5, we see a rise in $R''_{conv-simul}$ with increasing W_{CP} – indicating better convective cooling at thinner channels with low hydraulic diameter. This has also been captured accurately in the expression for $R_{conv-theory}$ as seen in Eqs. (37)–(39). Interestingly we see a weak increase of $R''_{conv-simul}$ with H_{CP} which goes against what is predicted by $R''_{conv-theory}$ in Eqs. (37–(39) which predicts a weak decrease in R_{conv} with increasing H_{CP}. It is to be remembered that from the previous paragraph that, $R''_{conv-simul}$ captures only the local convection at the roof of the microchannel (according to Eq. (34)) and is not an actual representation of the total area averaged convection coefficient. It is also an overestimation of the actual R_{conv} since it is defined based on the hottest part of the microchannel, $T_{CP\ microchannel\ roof}$. The impingement or convection coefficient at the roof of the channels decreases with increasing H_{CP} and the roof is also closer to the heated surface at larger H_{CP}. These two reasons combined explain the general rise in $R_{conv-simul}$ with H_{CP}. H_{CP} however much more strongly affects the conduction component, R_{cond} as given by Eq. (41). Studying the relative magnitudes of these resistance components are important – they provide us key insights into designing better coolers. In designs with low H_{MF}, of 75 μm, it has been seen that $R_{cond-simul}$ dominates over $R_{conv-simul}$, indicating that further improvements in those cooling devices should come from reducing the Silicon thickness between the cooling channels and hotspot rather than attempting to improve convective capability. This simultaneously bolsters the need for embedded cooling technologies that aim to directly etch microchannels on the backside of hot chips and reduce R_{cond} as much

as possible use in extreme heat flux next generation power dense electronics. The best performing design shows a total thermal resistance, R_{total} of 0.05 cm^2-K/W. This MMC will be capable of removing more than 1400 W/cm^2 of heat flux without exceeding average chip temperature of 100 °C. The worst performing design showed R_{total} around 0.085 cm^2-K/W, which would also be able to dissipate 850 W/cm^2 flux without exceeding 100 °C $T_{chip-avg}$.

Next, we focus on simulation results. Note that every device geometry has a different volume and thus has been simulated with different mass flux going through it. The different mass flux, m_{MF} values calculated as Eq. (5), which assumes an equivalent full device (area L^2) flow rate of 0.2 lpm. Since the total device flow rate (0.2 lpm) and heat flux (800 W/cm^2) was kept constant across all the designs, average temperature of the heater surface ($T_{chip-avg}$) was a direct measure of the device thermal performance. Device total thermal resistance is related to chip average temperature linearly, as $R''_{total-simul} = (T_{chip-avg} - T_{water-in})/q''$. To make analysis easier the 54 total geometries are first broken into two sets of 27 geometries based on their manifold heights – H_{MF}700 and H_{MF}1500. In this section, we report and analyze only the 27 geometries in the H_{MF}700 range. The effect of variation in W_{CP}, H_{CP} and W_{MF} in the other 27 geometries of the H_{MF}1500 set were verified to be consistent with H_{MF}700 set geometries. (See Supplementary Information fig. A3 for H_{MF}1500 plot)

Fig. 6 comprehensively plots the 27 geometries in the H_{MF}700 set. Fig. 6(a–c) shows variation of chip average temperatures and (d–f) shows variation in device pressure drops as a function of the three geometric parameters, W_{CP}, H_{CP} and W_{MF} respectively. Fig. 6(g–l) are double bar plots that attempt to quantify the percentage change in chip temperature and pressure drop values respectively, as these geometric parameters were slowly increased from the lowest value. Higher values of these percentage changes (taller bars) associated with a geometric parameter indicate that it strongly affects the thermal and hydraulic performance of the overall device.

From Fig. 6(a) we see an overall rise in $T_{chip-avg}$ with increasing W_{CP}. Changing W_{CP} doesn't affect the conduction resistance, $R''_{cond-theory}$ and thus variations because of changing these parameters are purely dominated by convection resistance. Increasing H_{CP} or reducing W_{CP}, both increase α and contribute to lowering thermal resistance and $T_{chip-avg}$. This is captured in the expression of $R_{conv-theory}$ in Eqs. (37) and (38). Increasing H_{CP} simultaneously reduces the conduction resistance, $R_{cond-theory}$ by reducing proportionally the amount of solid silicon between the hot chip and the fluid CP channels (Eq. (41)). Conduction resistance often dominates over convection in the overall resistance as seen from Fig. 5. These behaviors are observed clearly in Fig. 6(a,b), where $T_{chip-avg}$ rises with increasing W_{CP} and decreasing H_{CP}. The outliers in these plots are the designs ($15W_{CP}-225H_{CP}$) and ($15W_{CP}-375H_{CP}$), which have extreme CP channel aspect ratios of 15 and 25. These will be discussed later in the Section. Bar plots in Fig. 6(d,e) also shows that the W_{CP} variation affects $T_{chip-avg}$ more strongly (showing > 7–10% change in $T_{chip-avg}$ with changing W_{CP} in many designs) than H_{CP} variations ($\sim$ 5–7% change in $T_{chip-avg}$ with changing H_{CP}).

The effect of W_{MF} on $T_{chip-avg}$ is much more complicated and harder to understand. Theoretically calculated W_{MF} shows a weak dependence as seen in Eqs. (37) and (38), $R_{conv,theory} \sim (W_{MF-wall} + W_{MF})^{1-x}$, predicting an overall rise in $T_{chip-avg}$ with increase in W_{MF}. This is seen clearly Fig. 6(c). The weak dependence results from two opposing effects that happen on changing W_{MF}. Increasing W_{MF} increases the mass flow per CP channel which tends to reduce R_{conv} and improve convection, but it also increases the total flow length within the CP which tends to worsen thermal performance. The outlying designs again are the same ones from Fig. 6(a,b), the extremely high α designs - ($15W_{CP}-225H_{CP}$) and ($15W_{CP}-375H_{CP}$). It is however important to note that these theoretical estimates still fail to capture the effect of flow maldistribution by the MF among all the CP channels – a factor that will also impact the thermal performance to a certain degree. The weak dependence of $T_{chip-avg}$ on W_{MF} was captured in the bar plot in Fig. 6(i) which shows that increasing W_{MF} causes < 5% change in $T_{chip-avg}$.

The designs which are off-trend and show outlying behavior in Fig. 6(a–c) are the ones with extreme aspect ratio, α values for the CP channels, $15W_{CP}-225H_{CP}(\alpha = 15)$ and $15W_{CP}-375H_{CP}(\alpha = 25)$. In these very high aspect ratio CP channels, the theoretical estimates for R_{conv} breaks down and another factor starts dominating – liquid starvation and improper impingement at the CP channel roof. The fluid turning from the MF side encounters high viscous resistance from the thin channels (15 μm W_{CP}) while it attempts to traverse the large depth of the CP, H_{CP} (225 and 375 μm) and impinge at the roof of the microchannel. This causes a severe deterioration of the convection capacity at the CP, and a massive jump in R_{conv}. Additionally, when the W_{MF} is also low (100 μm), then the $\dot{m}_{CP}$ is also low – this causes an even further worsening of cooling capability. The high R_{conv} now dominates over the R_{cond} which is lowered due to increased H_{CP} and leads to high overall resistance, R_{total}. This is observed in the design $100W_{MF}-15W_{CP}-375H_{CP}$. Mass flux per CP channel is proportional to the fluid velocity and heat transfer coefficient at the channel roof is directly related to the velocity gradient – thus observing the fluid velocity profile will give us an insight into the convective cooling at the CP. Fig. 7(a) clearly shows that the velocity gradient reduces as H_{CP} increases. Design $100W_{MF}-15W_{CP}-375H_{CP}$ shows extremely low velocity (low mass flux because of low W_{MF}) and velocity gradient magnitude (for H_{CP} of 375 μm) at the CP channel roof and thus high $T_{chip-avg}$ (Fig. 7(d)). Increasing $\dot{m}_{CP}$ by increasing W_{MF} can alleviate this liquid starvation issue at the CP channel (Fig. 7(c),(f)) and improve performance. Increasing W_{CP} also increases $\dot{m}_{CP}$, simultaneously reduces α values and improve the gradient of velocity at the CP roof. This was also observed visibly in Fig. 7(b), where W_{CP} has been increased to 50 and 90 μm, also showing improvement in cooling performance (lowered $T_{chip-avg}$ in Fig. 7(e))

Next, we look at the total device pressure drop variation with changing W_{CP}, H_{CP} and W_{MF}. The pressure drop component from the CP and MF side are noted in Eqs. (9) and (13), in the previous section "Novel Two-level vs Conventional Single-level Manifold". ΔP_{CP} scales inversely with W_{CP} and H^2_{CP}, indicating that increase in W_{CP} and H_{CP} will cause lowering of pressure drop. Changing W_{CP} and H_{CP} doesn't affect ΔP_{MF} which makes understanding the pressure drop variations easier. This is observed clearly in Fig. 6(d,e). The percentage changes in ΔP on increasing W_{CP} and H_{CP} are of similar levels (as seen from the bar plots in Fig. 6(j,k)). This observation is also intuitive because increasing W_{CP} and H_{CP} both lead to increased cross-sectional area available for the flowing fluid – thus lowering viscous flow resistance. The dependence of ΔP on W_{MF} is slightly more complicated since W_{MF} affects both the MF and CP side pressure drop in opposing ways, $\Delta P_{CP} \sim (W_{MF-wall} + W_{MF})^2$ and $\Delta P_{MF} \sim \frac{W_{MF-wall}+W_{MF}}{W^2_{MF}}$. These opposing effects are observed because increasing W_{MF} causes reduction in ΔP_{MF} by increasing cross section of the MF but also increases $\dot{m}_{CP}$ and $L_{flow-CP\ bridge}$, thus causing increase in ΔP_{CP}. The percentage contribution of ΔP_{CP} and ΔP_{MF} on the overall ΔP_{total} also affects this variation. This is captured accurately in Fig. 6(f), where some designs show increase while others show reduction in ΔP_{total}. The percentage variation bar plot (Fig. 6(l)) shows less change in ΔP_{total} with increasing W_{MF} because of these competing effects on ΔP_{CP} and ΔP_{MF}.

Figs. 8 and 9 attempts to understand the effect of the final parameter, H_{MF}. Increasing H_{MF} reduces the MF flow cross-section area and helps to reduce ΔP_{MF} immensely as seen in Fig. 8(b).

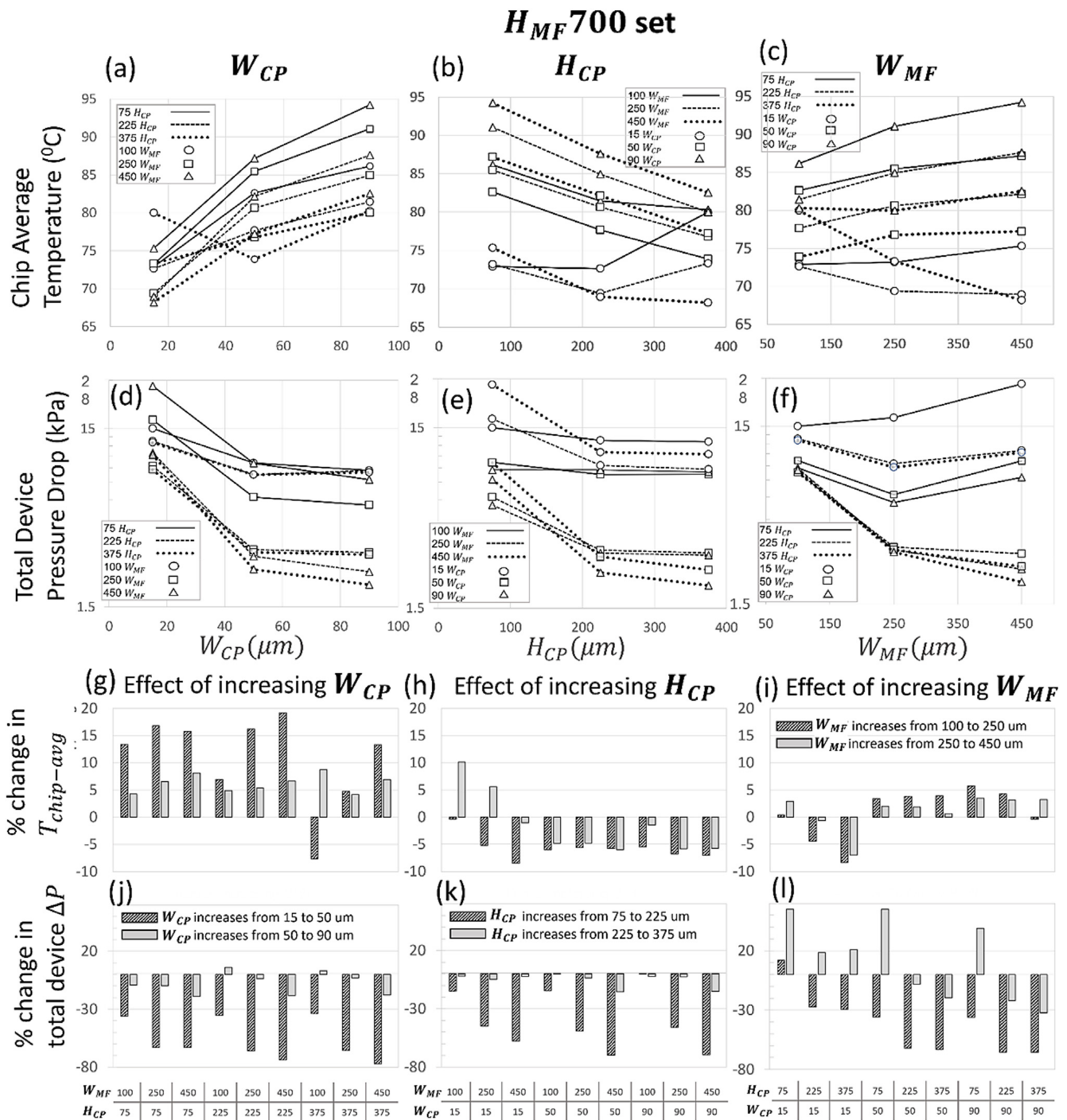

Fig. 6. The effect of changing pertinent geometric parameters on thermo-fluidic performance of 3DMMCs for the 27 geometries with 700 H_{MF}. (a) Effect on chip average temperature and (d) ΔP on increasing W_{CP}. (b) Effect on temperature and (e) ΔP on increasing H_{CP}. (c) Effect of increasing W_{MF} on temperature and (f) ΔP. (g) Percentage change on temperature and (j) ΔP on increasing W_{CP} sequentially from 15 to 50 μm and then 50 to 90 μm. (h)% change on T and (k) ΔP on increasing H_{CP} from 75 to 225 and then 225 to 375 μm. (i)% change in T and (l) ΔP on increasing W_{MF} from 100 to 250 μm and then 250 to 450 μm.

The cooling capability at the CP is not that affected by H_{MF} – the same amount of cooling fluid is still passing through the same numbers and dimensions of CP channels, thus keeping $T_{chip-avg}$ almost the same. We see this in Fig. 9(a,b) – showing only 2–5% increase in overall $T_{chip-avg}$ as H_{MF} increases. This deterioration in $T_{chip-avg}$ happens at larger H_{MF} because pressure levels in the MF side are lower and causes stronger flow maldistribution within the different CP channels. This has been confirmed by plotting peak velocity values at the different CP channels for all the designs. One such representative plot is shown in Fig. 8(c) for the design $100W_{MF}-90W_{CP}-225H_{CP}$ for two different H_{MF}, clearly showing maldistribution in the larger H_{MF}. This flow maldistribution also strongly affects the temperature map on the chip, which can be characterized by temperature non-uniformity and plotted in Fig. 8(a), given as –

$$Non-uniformity = \frac{T_{chip-max} - T_{chip-avg}}{T_{chip-avg}} \tag{43}$$

The non-uniformity was seen to be higher for the cases with a low W_{MF} of 100 μm, which was also accompanied by low $\dot{m}_{CP}$. For overall lower values of $\dot{m}_{CP}$, the effect of flow maldistribution is stronger, causing more temperature non-uniformity.

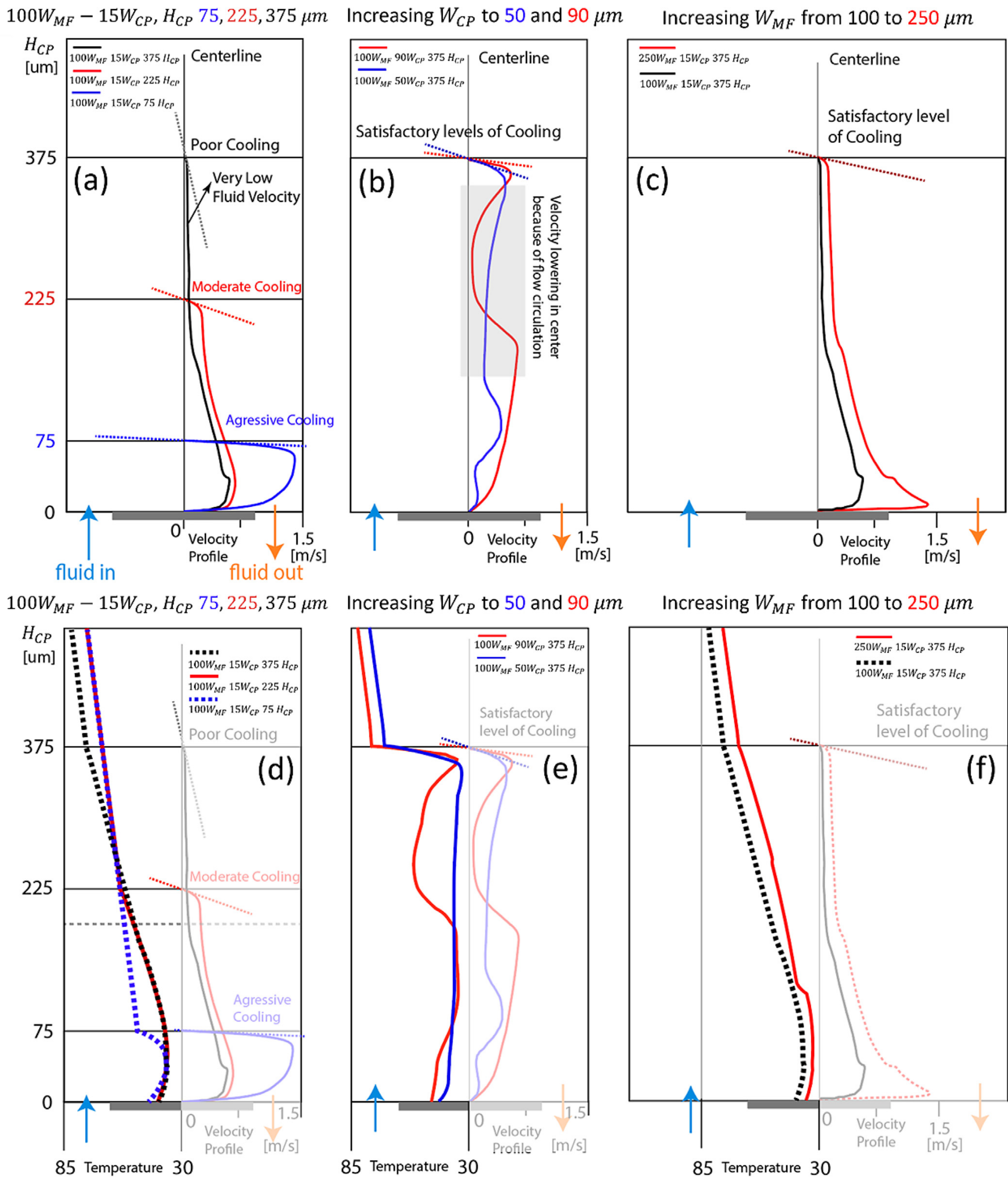

Fig. 7. Schematics that plots fluid velocity and temperature in one of the central channels of the SMC models to explain erratic behavior of 15 W_{CP} channel geometries. (a) $100W_{MF}$-$15W_{CP}$ geometries have low $\dot{m}_{CP}$ and fluid starvation issues arise in the extreme aspect ratio (H_{CP} 225 and 375 μm) geometries. As H_{CP} increases, the near wall velocity gradient drops drastically from $75H_{CP}$ (blue, high, aggressive cooling) through $225H_{CP}$ (red, medium, moderate cooling) to $375H_{CP}$ (black, very low, extreme fluid starvation) – fluid starvation issue at higher H_{CP} dominates over the lowered conduction resistance in the thinner Silicon wall, this plot should be seen together with (d) which plots the fluid temperature along the center of the same channel. The very low velocity sections in the $100W_{MF} - 15W_{CP} - 375H_{CP}$ channel geometry also shows a corresponding drastic rise in temperature (black dotted line). (b) These shows how increasing W_{CP} from 15 to 50 and 90 μm, increases $\dot{m}_{CP}$ and fixes the fluid starvation issue – this is observed in higher near wall velocity gradient (and an (e) accompanied trend in temperature), (c) The other way to fix this starvation issue is to increase W_{MF}, thus reducing number of MF channels and thus indirectly increase the mass flux per CP channel. This is plotted as velocity and (f) temperature plots. Even though in (c) absolute velocity value in the $250W_{MF} - 15W_{CP} - 375H_{CP}$ case is not much higher than $100W_{MF}$ case, the $250W_{MF}$ case velocity profile manages to obtain a much higher near wall gradient – this causes a significantly higher cooling effect as compared to the $100W_{MF}$ case. The $250W_{MF}$ cases do not show any fluid starvation issue.

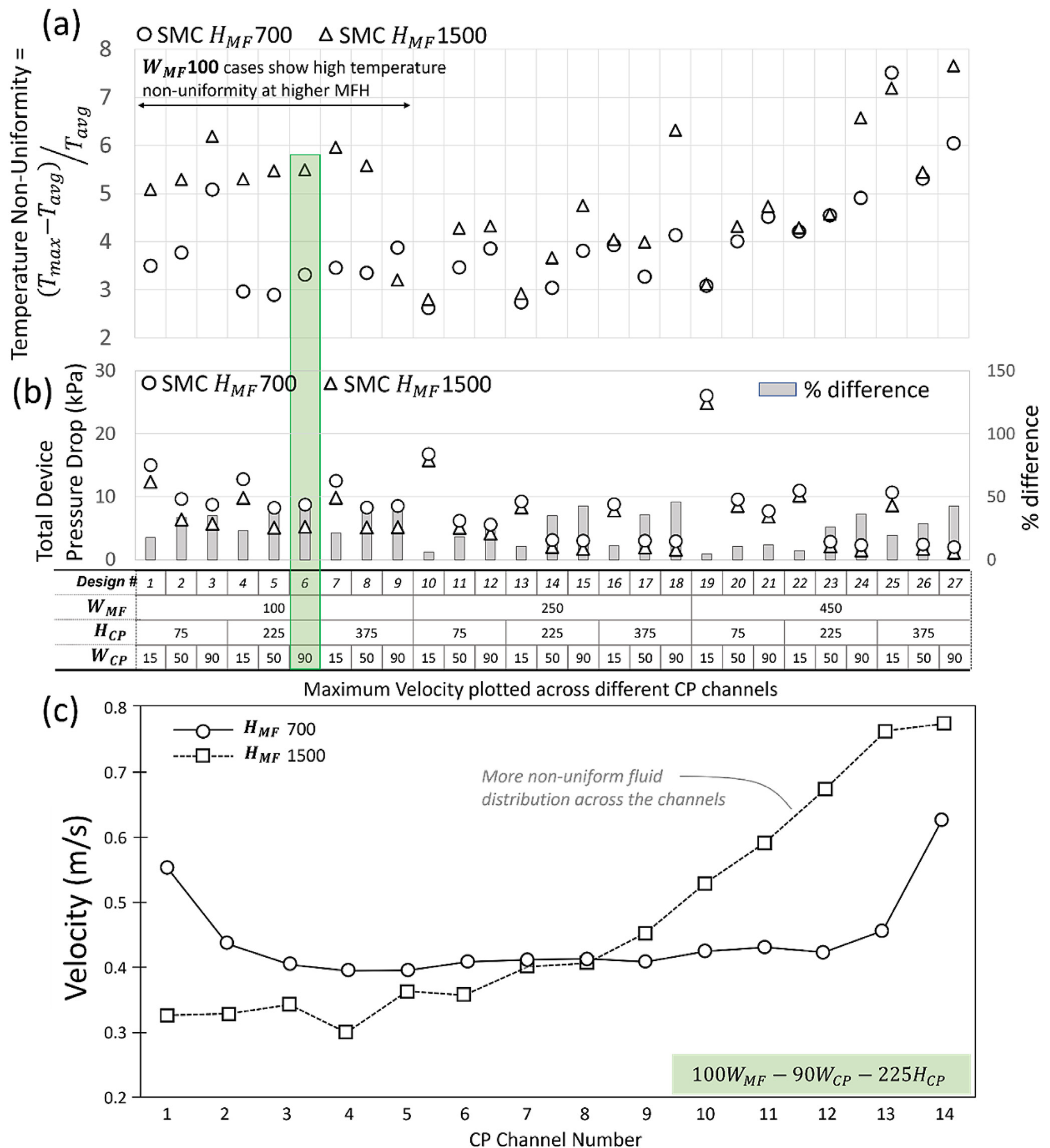

Fig. 8. (a) Plot showing chip temperature non-uniformity between sample sets of H_{MF}700 (circles) and H_{MF}1500 (triangles). (b) Plot showing device pressure drops. The higher non-uniformity of the temperature is larger for H_{MF}1500 cases – this is the result of exacerbated fluid maldistribution issues between the CP channels at higher H_{MF} values. (c) One such plot is shown for the highlighted (green) sample where the maldistribution issues are clear. The non-uniformity issues are also higher for the $100W_{MF}$ cases, the samples which already have low fluid velocity per CP channels.

2.3. SMC vs SCPUC simulation results

Fig. 9 additionally lists the 27 SCPUC simulations that were performed as a comparison model to the SMC simulations. It shows that the SCPUC model significantly overpredicts chip average temperature when W_{CP} is large. This overprediction is often as high as 25% (9 designs) to 45% ($100W_{MF} - 90W_{CP} - 75H_{CP}$ design). To investigate this further, we present the flow pattern images from within the CP microchannel for both the SMC and SCPUC models. As observed in the Fig. 10, the flow streamlines within the CP channels of the SMC model is characterized by the flow turning by 90° as it flows from the MF to the CP. This flow turning is also accompanied by a flow acceleration effect as the fluid crashes against the further side of the CP channel (Fig. 10(l,m)), then swirling up and towards the outlet. The vortices and swirling effect within the CP channels increase near wall fluid velocity, and thus local heat

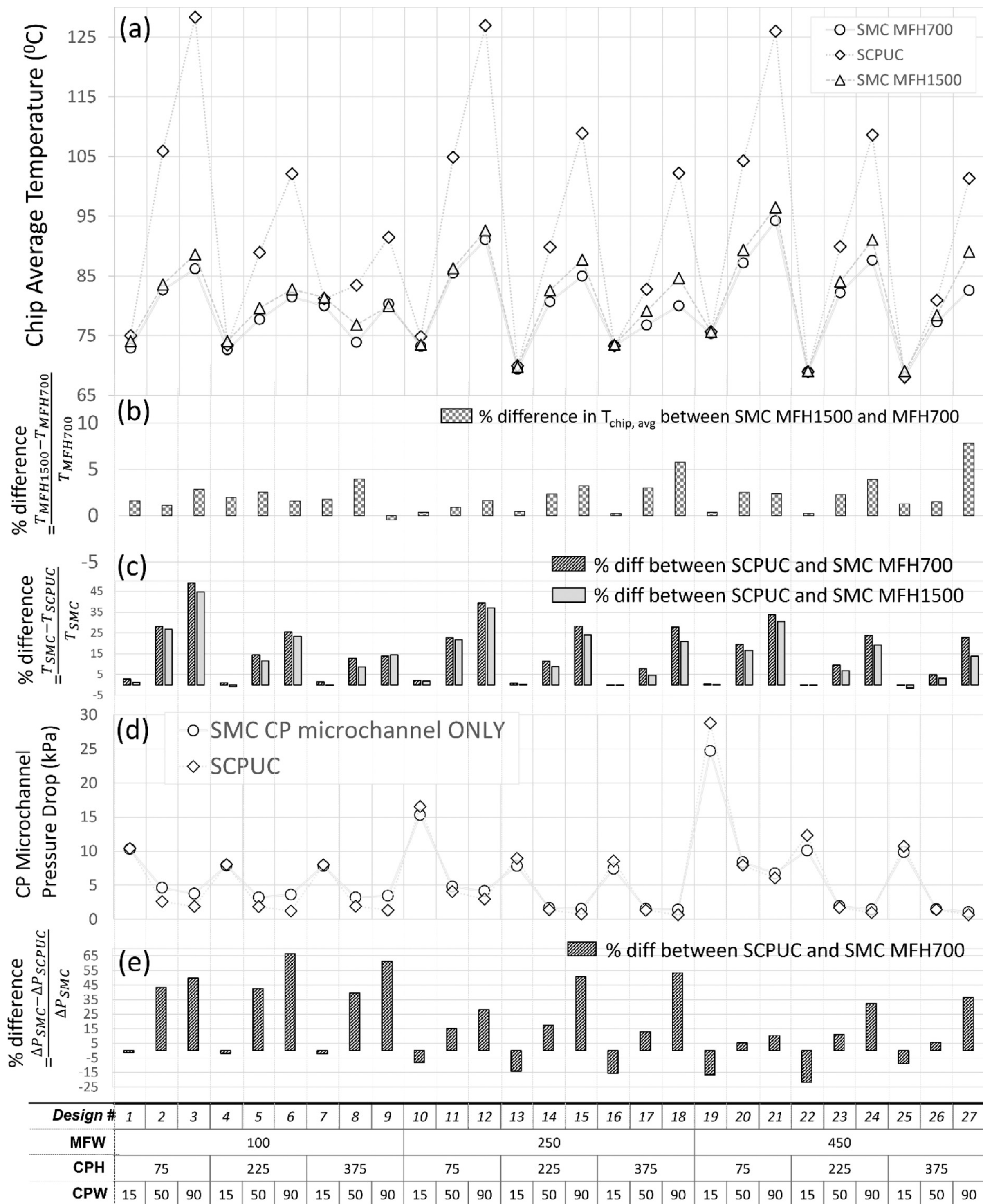

Fig. 9. A plot comparing three sets of data – 54 SMC model results for geometries of $H_{MF}700$, $H_{MF}1500$ and 27 for SCPUC model for the same geometries. (a) Chip average temperature plots, (b)% difference to capture effect of H_{MF} change by plotting SMC model simulations between $H_{MF}700$ and $H_{MF}1500$ cases. (c) Large percentage error in the SCPUC model predictions as compared to SMC model predictions (d) ΔP comparison between CP sections of $H_{MF}700$ simulations and SCUPUC simulations and (e) corresponding% difference in ΔP s predictions.

transfer coefficient in several sections. On the other hand, in the SCPUC simulations, fluid has been introduced uniformly at the entrance of the CP channel; this fails to capture this swirling motion of the fluid. This is the primary reason for the massive overprediction of chip temperature by the SCPUC model simulations. However, SCPUC model thermal predictions are very close to the SMC model predictions for the small W_{CP} (15 μm) cases. This happens since the smaller confines of the CP channel make it impossible for the swirling motion to develop effectively (Fig. 10(b)), and thus for low W_{CP} (15 μm) cases, flow within the SMC and SCPUC model CP channels closely resemble each other (Fig. 10(a–e)). This finding additionally establishes that flow swirling within CP channels is one of the most important flow phenomena that leads to superior thermal performance of 3DMMC type coolers even when W_{CP} is much larger. This is a purely geometric effect and develops because of the 90° angled turning from the MF to the CP. SCPUC

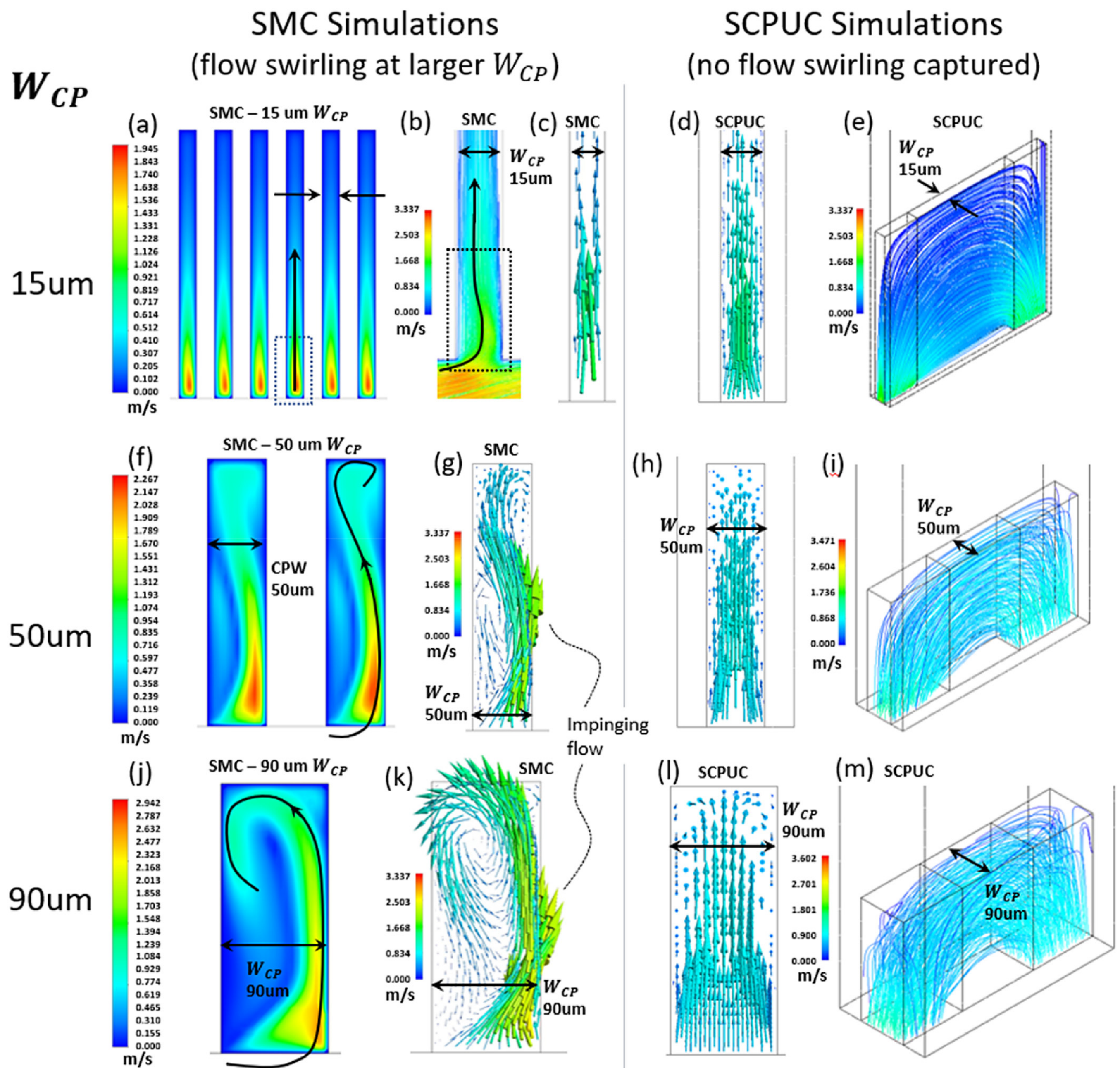

Fig. 10. Flow swirling effect as the fluid turns 90° from the MF to the CP is captured by the SMC model but not by the widely popular SCPUC model. (a) SMC simulation of 15W_{CP} cases have very narrow channels and they suppress any flow swirling. (b) Zoomed in view of one of the channels to show that the flow swirling doesn't develop. (c) SMC model simulations show straight flow vector from MF to CP. (d) For comparison, SCPUC simulation shows very similar straight flow in the CP. (e) Isometric view showing straight flow in the 15W_{CP} channel. (f) Flow swirling effect starts to show up at larger W_{CP} (50 μm) for SMC simulations and corresponding (g) single channel flow vectors. (h) For comparison, SCPUC simulations with 90 μm W_{CP} do not show any swirling behavior and have straight flow. (i) Isometric view of 90 μm W_{CP} as captured by the SCPUC model. (j) SMC simulation of 90 μm W_{CP} channel showing strong swirling effect with isometric views in (l) and (m). Compare these directly with (i) SCPUC model which shows no swirling.

model simulations which have been used extensively by previous researchers [4,14,19–26] can capture none of these effects, and thus, should not be employed to make absolute predictions about thermal performance for 3DMMC coolers especially when W_{CP} is larger than ~10 μm. This flow swirling is not captured in expressions for $R''_{conv-simul}$ and further bolsters our claim that $R''_{conv-simul}$ is not a true representation but rather always an overestimation of the actual R_{conv} within the device.

The ΔP predictions in the CP microchannel also follow a similar trend – the SCPUC and SMC model predictions are close to each other for the W_{CP} 15 μm cases because the flow profiles are similar to each other, while they get worse for the larger W_{CP} cases where the effects of flow swirling become dominant. Flow swirling is only captured by the SMC model; it is inherently a fluid acceleration or impinging mechanism and causes the ΔP_{SMC} to be larger than ΔP_{SCPUC} (Fig. 10(d,e)).

The COPs of all the devices are also plotted in Fig. 11(b), which is given by the ratio of energy flux supplied by the heater and energy expended (pump power) to force the fluid through the cooler. Surprisingly, we observe that the best performing device (15W_{CP} designs) do not provide the highest COP. This is the result of the exponentially large ΔP associated with the low W_{CP} de-

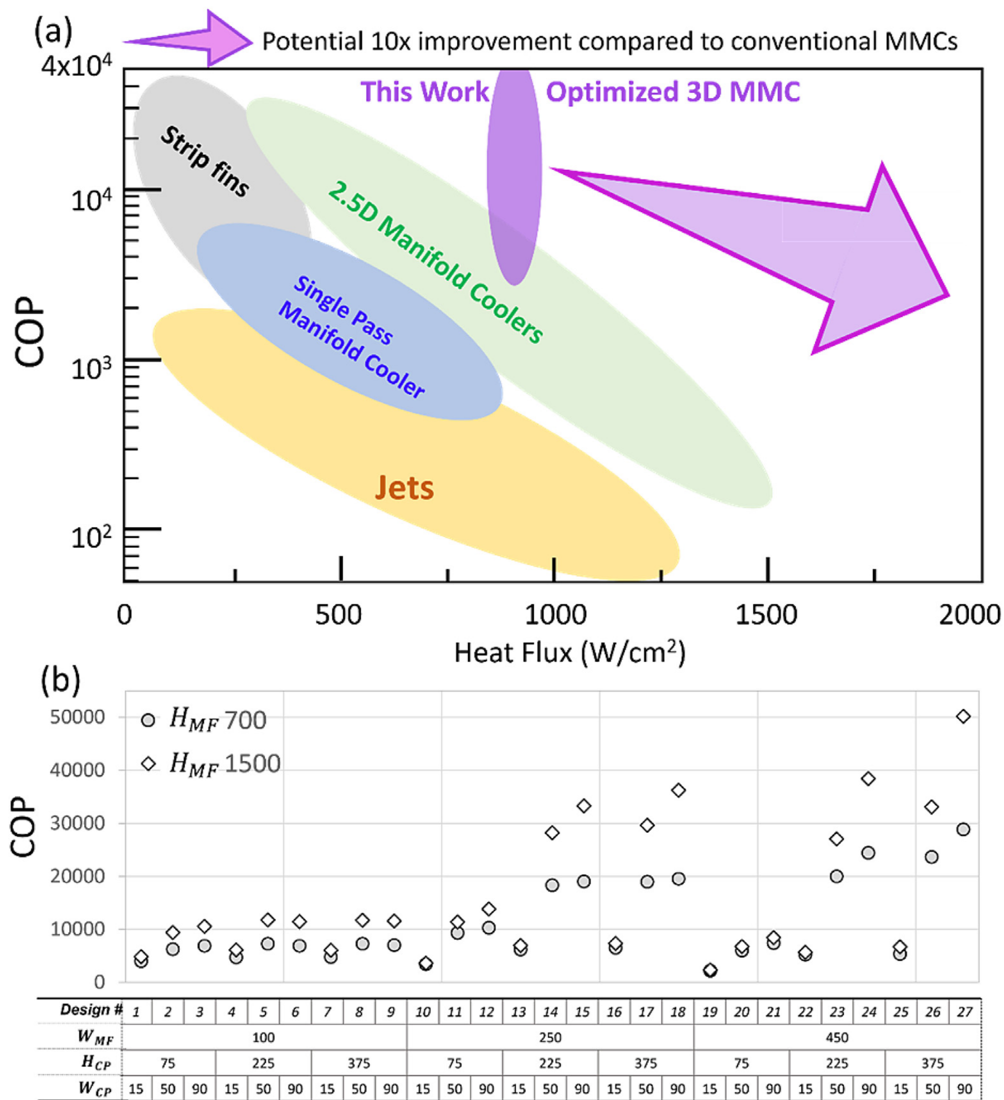

Fig. 11. Different types of existing cooling technologies (Data for conventional coolers are adapted from van Erp et al. [7]) plotted across two different metrics COP and Heat Flux, both of which need to be maximized. A pareto optimality exists between these two parameters, where any effort to increase heat flux is also accompanied by a drop in COP. Although, our multi-level 3DMMC coolers show a potential for more than 10x improvement in cooler COP at 1 kW/cm^2 heat flux level as compared to traditional single-level manifolds. The purple circle summarizes the COP values observed at 800 W/cm^2 heat flux and 0.2 lpm full device level flow rate for all the 54 geometries simulated. The arrow represents the expected behavior of these designs at higher heat flux levels.

signs, thus driving up the input pump power. Thus, higher COPs ($>$ 20,000) are observed for the slightly larger 50 and 90 μm W_{CP} designs combined with 225 and 450 μm W_{MF} cases. Also, we see higher COPs for the $H_{MF}1500$ set compared to their $H_{MF}700$ counterparts – this is intuitive because we always observe lower ΔP associated with the taller manifolds in the $H_{MF}1500$ set. The highest COP of 50,144 was observed for the $W_{MF}450 - H_{MF}1500 - W_{CP}90 - H_{CP}375$ design which has a chip average temperature of 82 °C compared to 68 °C in the best thermal performing design, $W_{MF}450 - H_{MF}700 - W_{CP}15 - H_{CP}375$. However, the best performing design had almost an order of magnitude lower, COP of 5380. This further bolster how merely reducing convection thermal resistance is not the best way to go about optimization of a 3DMMC, since several important geometric parameters combined (both on the MF and CP side) determines the device efficiency (COP). Additionally, COP of 50,000, which can only be achieved through a 3DMMC configuration shows a massive 5× improvement over the best performing single-level manifolded coolers at extreme heat flux levels (Fig. 11).

3. Conclusion

In this letter, we detailed a 2-level 3D Manifolded Micro-Cooler (MMC) design which shows potentially 2–2.5 times improvement in COP as compared to its single-level MMC counterpart. Then we simplified the complicated 2-level 3DMMC design into a reduced order model considering ¼th of a set of single Manifold Inflow and outflow channels (SMC model). The SMC model was first validated against quarter model simulations [16–18] which is closest to the exact simulation of the full geometry, which showed the capability of the SMC model to predict the thermal performance of these coolers with less than 5% error, even when the size of the heater footprint increases 16 times (25–400 mm^2) but keep simulation expense low. This also enables fast and wider probing of design spaces to optimize such 3DMMC designs. 54 simulations were performed by setting up a small design of experiment around the most important geometric parameters, Manifold channel width and height, and CP channel width and height. W_{CP} was found to be the most important parameter in determining

thermal performance followed by H_{CP}. W_{MF} determines fluid redistribution within the CP and indirectly control thermal performance. Increase in H_{MF} causes massive improvement in COP without much worsening thermal performance. Simple theoretical dimensional dependances were derived, which were not useful for absolute prediction but captured the variations of thermo-fluidic performance with changing geometric parameters, quite satisfactorily. The SMC model results were further compared against widely used CP Channel Model (SCPUC) [4,14,19–26] to show that these CP channel models were oversimplified and grossly underpredict device thermal performance level especially when the CP width is > 50 μm. The reason for this massive (often up to 65%) underprediction was found to be recirculations and vortices generated by flow swirling from the Manifold at 90° angle into the CP, which is captured by the SMC model simulations but not by the SCPUC model. COP of the devices were reported. It shows the potential of 10x improvement in COP against conventional single-level Manifolded Coolers as seen in Fig. 11. The most optimized coolers found in this study will be able to dissipate > 1400 W/cm^2 heat flux without exceeding an average chip temperature of 100 °C.

Declaration of Competing Interest

None.

CRediT authorship contribution statement

Sougata Hazra: Conceptualization, Data curation, Formal analysis, Investigation, Methodology, Writing – original draft, Writing – review & editing. **Tiwei Wei:** Investigation. **Yujui Lin:** Investigation. **Mehdi Asheghi:** Conceptualization, Funding acquisition, Supervision, Writing – review & editing. **Kenneth Goodson:** Funding acquisition. **Man Prakash Gupta:** Conceptualization, Funding acquisition, Supervision, Writing – review & editing. **Michael Degner:** Funding acquisition.

Data Availability

Data will be made available on request.

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Supplementary materials

Supplementary material associated with this article can be found, in the online version, at doi:10.1016/j.ijheatmasstransfer.2022.123356.

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