IMPACT International Microsystems, Packaging, Assembly and Circuits Technology conference

Wafer Level Bumping Technology for High Voltage LED Packaging

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ABSTRACT

This paper proposed and developed an effective thermal management method for HVLED packaging with wafer level bumping technology. In the HVLED package, multiple thermal bumps were fabricated on HVLED chips to enhance heat dissipation. Cu-Sn-Cu bumps were used. The size, pitch and stand-off height of bumps were optimized for underfill dispensing. Moreover, a high thermal conductivity underfilll was used to further improve the thermal performance of the package.

INTRODUCTION

High-voltage light-emitting diode (HVLED) serves as a promising solution to reduce the current crowing and efficiency droop due to its high operation voltage and low driving current [1]. It also increases the light emission efficiency. The traditional die attach bonding method would not be suitable due to its high thermal resistance. Flip chip (FC) technology is an alternative solution for HVLED thermal management, which has been applied to LED packaging industry in the last decade. The flip chip bumps provide the mechanical support, electrical interconnects and thermal dissipation path. The bump density and geometry play important roles to the overall performance of the HVLED package. Nevertheless, the thermal performance may be even worse than the conventional LED with die attach adhesive if the bump layout is not properly designed [2]. A number of studies on the optimization of bump number and underfill thermal conductivity have been done to reduce the thermal resistance of LED flip chip packages [3, 4, 5]. However, they mainly focused on the Au bumps at the package level. In this study, we designed and fabricated an effective thermal management structure for HVLED packaging with wafer level bumping technology. Copper and tin bumps were used and were electroplated on the chip and silicon submount. Base on the Cu-Sn-Cu bonding solution, it is efficient to fabricate multiple thermal bumps for better heat dissipation. Also, it is possible to adjust the stand-off height of the flip chip assembly to optimize the thermal performance and underfill dispensing process. Moreover, the bumping process could be fabricated through wafer-level packaging process for high throughput and low cost manufacturing [6].

PACKAGE DESIGN

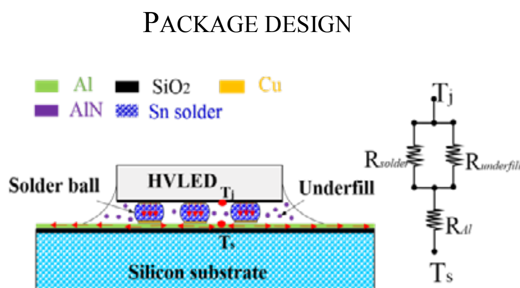

FIGURE 1 HEAT GENERATED AT THE JUNCTION OF HVLED FLOWS THROUGH THE PATH OF LEAST RESISTANCE

As shown by the thermal resistance network in Figure 1, the p-n junction is the origin of heat source and the hottest spot in a HVLED package. The network consists of two paths in parallel, namely, solder bumps and underfill [7]. Since the solder bumps are made of metal, which has higher thermal conductivity than underfill, they play the dominant role in heat dissipation.

As shown in Eq. (1) and (2), the heat flow $\boldsymbol{Q}$ has a close relation with thermal resistance **R,** where **R** is inverse proportional to the heat transfer area $\boldsymbol{A}$ and the thermal conductivity k, and proportional to the thickness $\Delta\boldsymbol{x}$.

$$\boldsymbol{Q}=\Delta\boldsymbol{T}/\mathrm{R} \tag{1}$$

where

$$\mathbf{R}=\Delta\boldsymbol{x}/(k\boldsymbol{A}) \tag{2}$$

Therefore, in order to reduce the thermal resistance of bonding between HVLED and its substrate, the height of the solder bumps should be reduced for decreasing $\Delta\boldsymbol{x}$, and the total number of bumps should be increased for enlarging $\boldsymbol{A}$. Moreover, the flip chip bonding structure should be enhanced by a high thermal conductivity underfill, which could also help to improve the heat dissipation of the package.

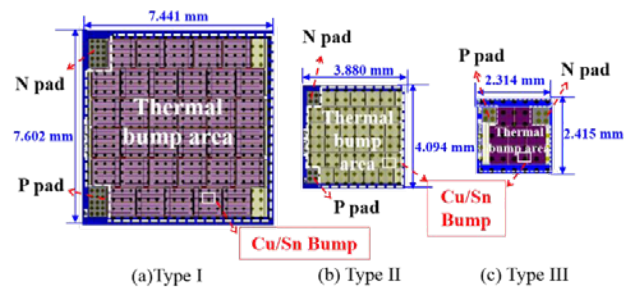

FIGURE 2 CU BUMPS LAYOUT ON THREE DIFFERENT TYPES OF HVLED

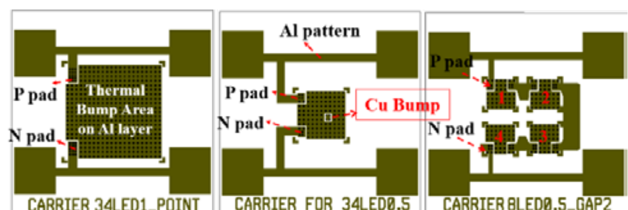

FIGURE 3 LAYOUTS OF CU-SN BUMPS ON SUBMOUNT CORRESPONDING TO THREE TYPES OF HVLED

Considering the thermal performance and filler size (0.4 - 1 μm) of a high thermal conductivity underfill, the bump pitch is set at 340 μm with a bump diameter of 150 μm. Figure 2 illustrates the bumps layout designed on three different types of HVLED. The HVLED chips are fabricated on an Epistar GaN-LED wafer and the peak wavelength was 470 nm [8]. For the design of the HVLED chip

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Type I, there were 34 LEDs, with the dimensions of 1 mm × 1 mm, in serial connection so as to construct an HVLED chip. For the HVLED with chip size of 3.880 mm × 4.094 mm, there were totally 34 LEDs with dimension of 0.5 mm × 0.5 mm, which cascaded together in an entire chip. The smallest HVLED chip with 2.314 mm × 2.415mm contains 8 LEDs with dimension 0.5 mm × 0.5 mm. The designed bump densities calculated by the ratio of bump area to chip area for the three types are 0.15, 0.13 and 0.16, respectively. The package layout contains two electrode areas and thermal bumps acting as the electrical contact and heat transfer path. The p-n metal contact area is located by bump arrays instead of one bulk bump since the high volume tin bump could be squeezed out and result in solder bridging. The corresponding silicon submount layout is shown in Figure 3.

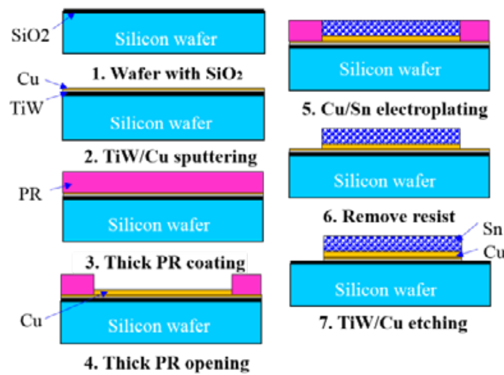

FIGURE 4 CU-SN ELECTROPLATING PROCESS FLOW ON HVLED CHIP

FABRICATION AND ASSEMBLY

In order to evaluate the flip chip bumping and bonding process for the HVLED, we have designed silicon dummy die and submount. The detailed schematic diagram of Cu/Sn electroplating process is elaborated in Figure 4. The thickness of silicon oxide is 500 nm, and the thickness of TiW/Cu is 50 nm / 500 nm. After fabricating the PR mold by photolithography process, the copper and tin are electroplated on the silicon substrate. The overall thickness of the copper and tin bump is controlled and determined by the PR mold thickness. Finally, the barrier layer TiW and seed layer Cu are removed through wet etching process with H_2O_2 and Cuprammonia, respectively. The optimized current density of Cu electroplating is 0.1ASD, and 0.08ASD for Sn electroplating.

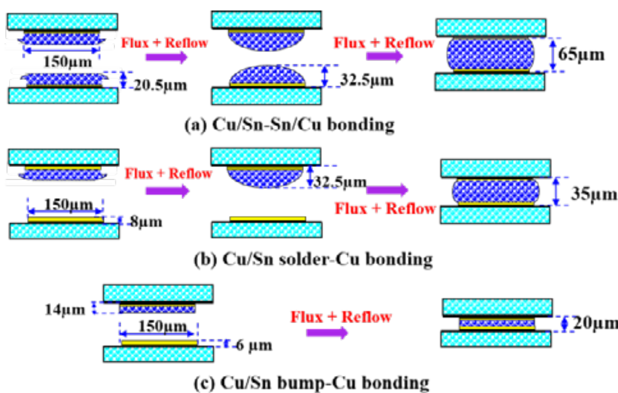

FIGURE 5 THREE TYPES OF BONDING METHODS

We have designed three types of bonding methods for evaluating the process window of underfill dispensing. Figure 5 shows the three bonding solutions with different stand-off heights. Figure 5(a) illustrates the stand-off height with 65 μm through Cu/Sn-Sn/Cu bonding. Tin bumps with 20.5 μm height are formed on both chip and submount after plating. The reflowed bump height is about 32.5 μm. Final assembly stand-off height is 65 μm. For the stand-off height of 35 μm shown in Figure 5(b), the tin solder on the submount is replaced by copper bond pad with a thickness of 8μm, and the reflowed tin solder bump on HVLED chip is still 32.5 μm high. For the stand-off height of 20 μm in Figure 5(c), Cu with 4 μm thickness and 10 μm thickness for Sn are electroplated on the HVLED while there is only 6 μm thickness Cu on the corresponding submount. In the following process, Cu-Sn-Cu bump bonding is realized through reflow process. For the three bonding solutions, the thickness of Cu-Sn could be easily controlled through electroplating process to develop the following underfill dispensing process.

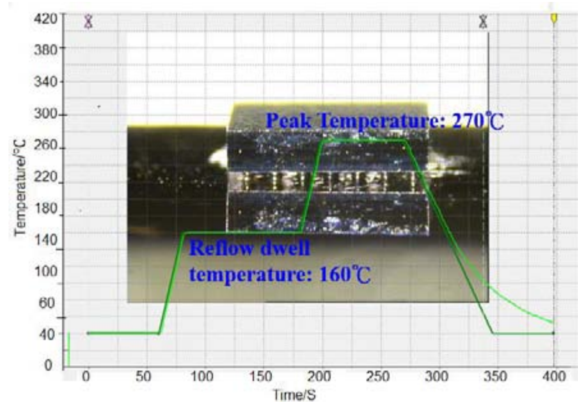

FIGURE 6 REFLOW PROFILE OF CU-SN-CU BONDING

Figure 6 shows the optimized reflow profile for Cu-Sn-Cu bonding. Before the reflow process, the flux ALPHA® WSX-FD is pre-dipped on the bump surface for the main purpose of removing metal oxidation. In order to achieve good bonding results without void inside the bonding interface, the reflow temperature and time are optimized experimentally. Finally, the reflow dwell temperature is chosen as 160 ℃ lasting for 100s to provide enough time for flux volatilization. The optimized peak temperature is 270 ℃ with 60s.

After fishing the bonding process, the underfill is dispensed with the three aforementioned stand-off heights. Compared with the bonding results and dispensing results, the bonding solution with stand-off height of 20 μm is chosen as the final package layout.

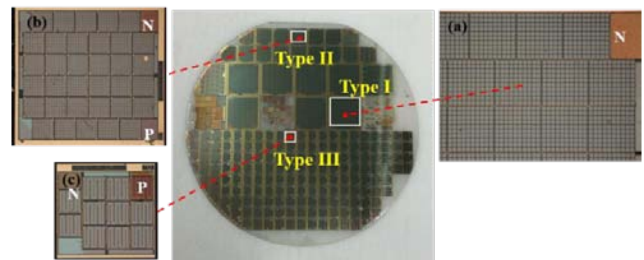

FIGURE 7 HVLED CHIP LAYOUT ON 2 INCH SAPPHIRE

The optimized package layout is used for HVLED packaging assembly and underfill dispensing. Figure 7 shows the chip layout with three different chip sizes on a 2 inch sapphire wafer. The p-n contact metal areas are exposed for electrical connection while other places are deposited with an insulation layer of SiO_2 to avoid short-

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circuit. For the wafer bumping process of the HVLED packaging, TiW/Cu is sputtered on the surface of sapphire wafer with HVLED chips. After PR mold through photolithography, the Cu-Sn bumps are electroplated on p-n contact areas and isolation areas. Figure 8 presents Cu-Sn bump fabrication results on different HVLED chip using the same configuration as dummy chip. After finishing the bumping process on sapphire, sapphire wafer backside grinding and polishing process are executed to leave 200 µm thickness for thermal dissipation and luminous efficiency consideration.

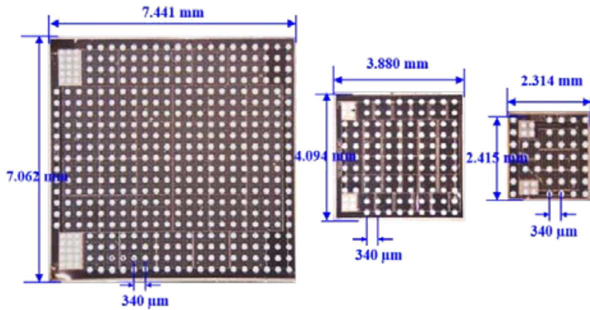

FIGURE 8 CU-SN BUMPING FABRICATION RESULTS ON HVLED CHIP

The Cu bumps fabrication on the silicon submount is the same as HVLED chip bumping process. The thickness of Cu bump is 6 µm with pitch 340 µm. After that, the HVLED chip with Cu/Sn bumps is flip-chip bonded on the silicon substrate through reflow process. Figure 9 shows the assembly results of HVLED chip and test substrate. For the fabricated silicon chip carrier in the figure, 4 HVLED chips with smallest chip size 2.314 mm × 2.415mm are connected in series for high luminance HVLED construction. Square Al pads located at four corners are designed for luminous efficiency measurement by ISP 500-100 Integrating Sphere test system.

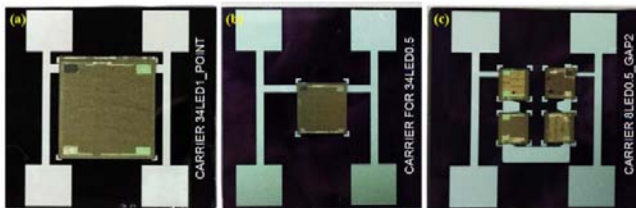

FIGURE 9 ASSEMBLY RESULTS OF HVLED CHIP AND TEST SUBSTRATE

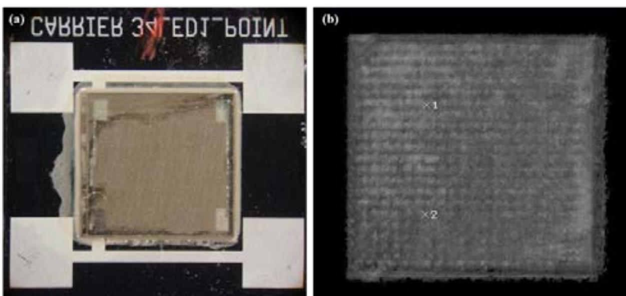

FIGURE 10 UNDERFILL FILLING RESULTS

Figure 10 gives the filling results of HVLED chip with large size after underfill dispensing. The underfill filling results are detected through C-SAM. The parameters of underfill dispensing including processing temperature, dispensing velocity are also investigated systematically to realize void-free. Moreover, the I-Pass edge route is chosen for underfill dispensing. The processing temperature is chosen as 80 ℃ to ensure that the gap under stand-off height 20 µm is fully filled.

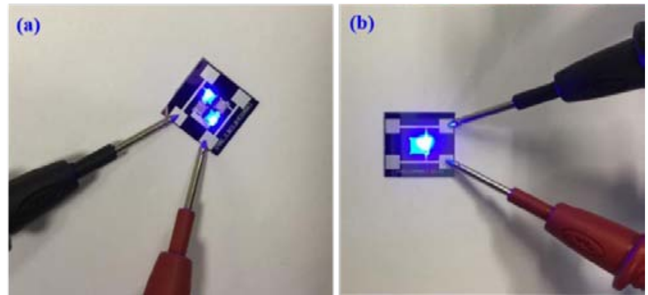

FIGURE 11 TEST RESULTS OF HVLED CHIP BASED ON CU-SN-CU BONDING

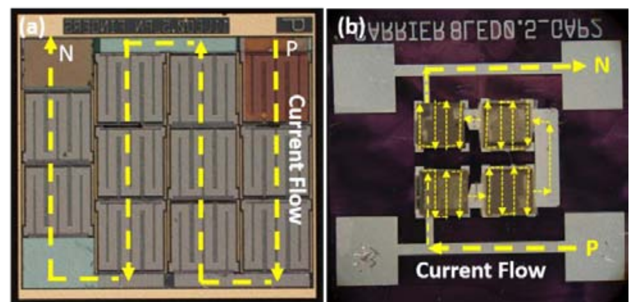

FIGURE 12 CURRENT FLOW OF ONE SINGLE HVLED CHIP AND ASSEMBLY CHIP CARRIER

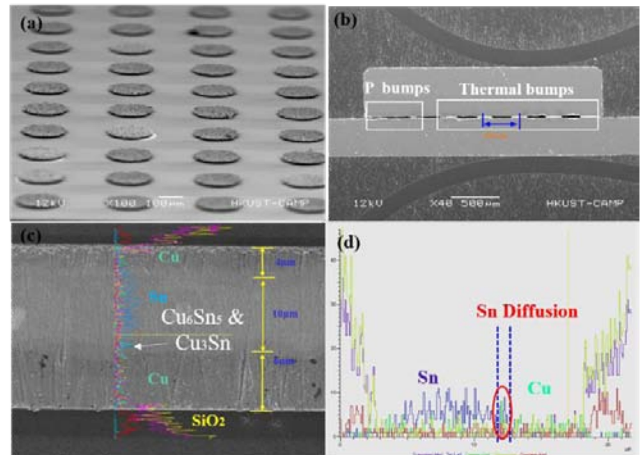

FIGURE 13 OPTIMIZED CU-SN-CU BONDING RESULTS: (A) ELECTROPLATED CU-SN BUMP; (B) CROSS-SECTION VIEW OF HVLED FLIP CHIP STRUCTURE; (C) CU-SN-CU BONDING RESULT; (D) EDX ANALYSIS OF CU-SN-CU BONDING

RESULTS AND DISCUSSION

After fabrication, the electrical connection is tested by inputting a current to light the HVLED. The electrical testing results are shown in Figure 11. According to the construction of HVLED chip shown in Figure 12, all the p-n junctions are connected with each other in series to achieve high voltage and performance. Therefore, all the LEDs could not work if Cu-Sn-Cu bonding problem under the p-n functional areas happens. In conclusion, although some HVLED

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chips could not work due to the yield of HVLED chip fabrication, the existed lighting LEDs prove that the Cu-Sn bump connection is workable and also present the feasibility of wafer bumping technology on sapphire wafer.

The bonding quality is inspected through SEM and EDX analysis. Figure 13 illustrates the cross section of optimized Cu-Sn-Cu bonding results, where no voids could be seen inside the bonding interface. The thin intermetallic compound (IMC) layer is formed between the interface of Cu and Sn bump with Sn diffusion. The thickness of IMC layer is measured about 2 µm. In addition, the die shear tests are performed to evaluate the bonding strength of Cu-Sn-Cu bonding. The average die shear strength with error bar is plotted in Figure 14, which is calculated from 10 samples for every chip size. The average die shear force for Type I HVLED chip 7.441 mm × 7.602 mm is 27.12 kg while the average die shear strength for Type III is 1.83 kg.

Moreover, the failure modes of the die shear test results are analyzed through SEM shown in Figure 15. The failure positions on HVLED and silicon submount show that the major fracture mode of Cu-Sn-Cu bonding is ductile fracture occurring through the Sn bump, which was regarded as the primary concern to ensure the mechanical reliability of HVLED packaging [9].

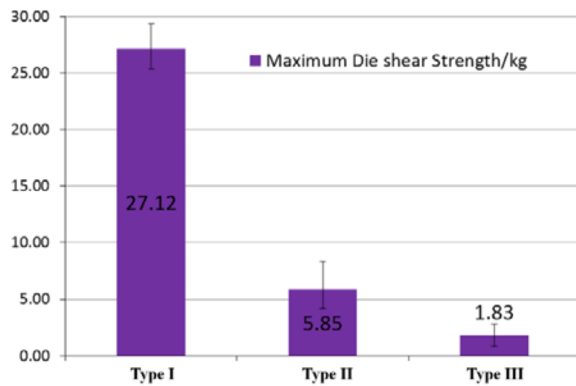

FIGURE 14 DIE SHEAR TEST RESULTS OF THREE KINDS OF CHIPS

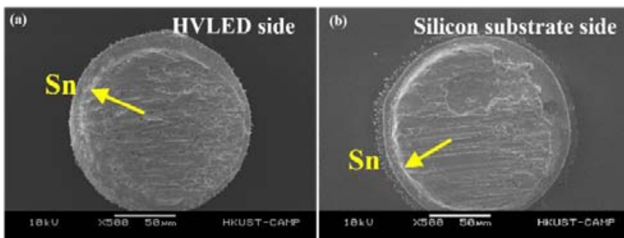

FIGURE 15 DUCTILE FRACTURE FAILURE MODE

CONCLUSIONS

In this paper, wafer level bumping process employed from IC packaging technology is implemented in HVLED packaging. Cu-Sn bumps were electroplated on the cascaded LED chips, providing electrical connection and thermal dissipation path. The parameters including height and pitch of Cu-Sn bumps were optimized for underfill dispensing. A robust bonding structure was achieved and the underfill was successfully dispensed under the flip chip structure with a stand-off height of 20 µm. The electrical characteristics, thermal resistance and luminous efficiency of the HVLED packaging will be measured and compared in the future work.

ACKNOWLEDGMENTS

This work was supported in part by a grant (T23-612/12-R) from the Research Grants Council of the Hong Kong Special Administrative Region Government under the Theme-Based Research Scheme, and by the Hong Kong's University Grant Committee via the Area of Excellence project AoE-P04-08. Moreover, the authors would like to thank Zhang Yu for making the underfill.

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