Thermal Analysis of Polymer 3D Printed Jet Impingement Coolers for High Performance 2.5D Si Interposer Packages

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ABSTRACT

Bare die liquid jet impingement cooling is an efficient cooling technique that has been successfully applied using various materials to create high performance cooling solutions. 2.5D Si interposer packages with several Si chips integrated side by side are a potential integrated solution for high performance systems. In this paper, we present the design, modeling, fabrication and experimental thermal characterization of 3D-printed impingement coolers applied to 2.5D Si interposer packages that contain two 8×8 mm^2 thermal test chips with integrated heaters and sensors. 3D-printing enables to use low cost materials for the cooler fabrication, to print the whole geometry in one piece and to customize the design to match nozzle array to the chip power map. The fabricated coolers have been applied to both lidless packages allowing the cooling solution to be directly applied to the backside of the chips, and to lidded packages that require a TIM between chip and lid. The thermal performance of the impingement cooler, including the chip self-heating and the thermal coupling, has been assessed for both package configurations using CFD simulations and experiments. A design of experiments of the TIM and lid properties has been performed to assess the trade-off of the beneficial and detrimental impact of the lid for different flow rates, in order to define guidelines for 2.5D interposer package thermal management solutions.

KEY WORDS: Liquid cooling, Si interposer, jet impingement cooling, 3D printing, lidless, TIM

NOMENCLATURE

A	chip area	ΔP	Pressure drop
$\dot{V}$	total flow rate	R_{th}	thermal resistance
W_p	total pump power	T_{in}	inlet liquid temperature
Q	total chip power		
d_i	Inlet diameter		
d_o	Outlet diameter		

Acronyms

PTCQ	Packaging Test Chip version Q
CFD	computation fluidic dynamic
FEM	finite element model
TIM	thermal interface material
BEOL	back-end of line

1. INTRODUCTION

Thermal management issues of 3D-TSV integration configurations are amongst the major challenges due to the thermal bottlenecks of the die-die interface materials with low thermal conductivities [1]. Alternatively, 2.5D Si interposer packages with multi-die integrated side by side, enable more cooling potential for applications combining high power components (logic, GPU, FPGA) and temperature sensitive components (DRAM, SerDes), which has potential for high performance systems with high-bandwidth and high-power applications [2]. The major thermal bottlenecks for conventional liquid cooling solutions are the presence of thermal interface material (TIM) and the lateral temperature gradient across the chip surface. The thermal resistivity of the most widely used TIM such as greases, gels, and phase-change materials (PCMs), can achieve 10 mm^2-K/W [3]. For the state of art nano-TIM, the thermal resistivity can be developed below 10 mm^2-K/W and even in the range of 1 mm^2-K/W with GE's copper nanospring [4]. However, it is also found that the interfacial thermal resistance (ITR) between TIM and heat sink can vary from 2 mm^2-K/W to 20 mm^2-K/W due to the mechanical compliance of the TIM [5].

Recently, several embedded cooling techniques without the use of the TIM have been applied on the 2.5D Si interposer packages. In [6] an embedded thermoelectric cooler (TEC) combined with silicon interposer for the electrical path is studied for hot spot cooling, but the power consumption of the TEC driver is a big challenge. In [7,8], microfluidic cooling delivery channels are embedded within an interposer package with high aspect ratio TSVs, and microfluidic chip I/Os. However, the I/O density is insufficient for high-bandwidth devices.

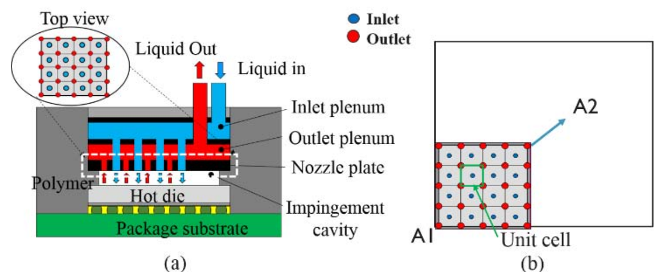

Figure 1. Scalable system of unit cells with single inlet and multiple outlets

Bare die liquid jet impingement cooling with locally distributed outlets has the advantage to overcome these problems since the liquid coolant can be directly ejected from the nozzles on the chip backside without TIM. The cooling efficiency is higher than the conventional jet impingement cooling with common outlets due to the absence of cross flow effects. Moreover, the jet cooling with cooling unit cell arrays enables hot spots targeted cooling with the customized nozzle pattern design. This cooling technique has been successfully applied using several fabrication techniques including Si Deep reactive-ion etching (DRIE) microfabrication [9], multilayer ceramic technology (MLC) [10] and LIGA (Lithography,

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Electroplating, and Molding) [11] or 3D printed metal [12, 13]. However, these solutions are very expensive.

In [14], we presented a chip level 3D-shaped polymer liquid jet impingement cooler. The schematic of this cooling concept is shown in Fig.1a, which indicates the main parts: inlet plenum, outlet plenum, nozzle plate and impingement cavity. The top view in Fig.1b shows the scalable approach of the unit cooling cells with a single inlet and multiple outlets, that can be used to cover the chip area. The cooler is designed for the 8×8 mm^2 thermal test chip, and contains a 4×4 inlet nozzle array with 600 µm diameter nozzles as shown in Fig.2a. It was demonstrated that polymer is a valuable alternative material for the fabrication of the impingement cooler instead of expensive Si based fabrication methods: modeling results show that it is not necessary to scale up the number of unit cells and to shrink the nozzle diameter accordingly to improve the thermal performance for a fixed cavity height [15], making the required diameters compatible with polymer fabrication methods. Moreover, the simulations indicate that the thermal conductivity of the cooler material has no impact on the thermal performance of the impingement cooler. The experimental characterization of this micromachined polymer cooler showed a very low thermal resistance of 0.25 K/W (0.16 cm^2-K/W) for a low pressure drop of 0.3 bar and good temperature uniformity across the chip surface.

In [16], we introduced the use of 3D-printing to fabricate polymer impingement coolers as shown in Fig.2b. 3D-printing enables to use low cost materials for the cooler fabrication, to print the whole geometry in one piece and to customize the design to match the nozzle array to the chip power map. Different versions of the impingement cooler have been designed and printed with nozzle diameters ranging from 300 to 800 µm. The cooler design with the finest nozzle diameters achieves a thermal resistance of 0.13 cm^2-K/W for a flow rate of 1000 ml/min. Benchmarking of the thermal performance of both demonstrators with literature data proved that cost-efficient polymer-based fabrication can be used to create a high performant chip level cooler with sub-mm nozzle diameters.

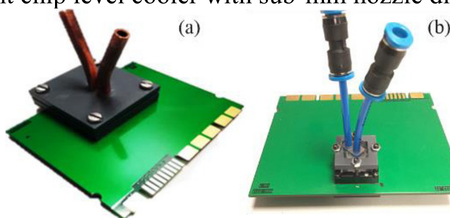

Figure 2. Photographs of the two coolers: (a) micromachined cooler [14] and (b) 3D printed cooler [16].

In this paper, we present the application of this cooling solution to 2.5D Si interposer packages, that contain two 8×8 mm^2 thermal test chips with integrated heaters and sensors as shown in Fig.3. Since bare die jet impingement cooling is a disruptive cooling technology requiring direct access to the backside of the Si chip, we also consider a less disruptive cooling implementation in which the impingement cooling is applied on the lid. The drawback of that approach is the significant thermal resistance of the TIM 1 between the chip and the lid. In order to estimate the extent of this detrimental impact of the TIM and lid and the overall thermal performance, coolers have been fabricated and characterized for both the lidless package allowing the cooling solutions to be directly applied to the backside of the chips, and for the lidded package that requires a TIM between chip and lid. This paper presents the design, modeling, fabrication, and experimental characterization of the 3D-printed impingement coolers applied to both packaging configurations. The first section of the paper (Section 2) presents the prototyping flow of the 3D printed jet impingement cooler including the design, the cooler fabrication, printing quality evaluation and cooler assembly process. In Section 3, the thermal performance of the fabricated coolers is experimentally characterized for the two packaging concepts. Moreover, the thermal impact of the lid and TIM is assessed for the bare die cooling and lidless cooling measurements. In Section 5, a hybrid modeling approach using conjugate heat transfer fluid dynamics simulations (CFD) and finite element modeling (FEM) based conduction modeling is introduced and experimentally validated. In Section 6, the hybrid modeling approach is applied for a design of experiments of the TIM and lid properties to assess the trade-off of the beneficial and detrimental impact of the lid for different flow rates.

2. 3D PRINTED COOLER DEMONSTRATOR

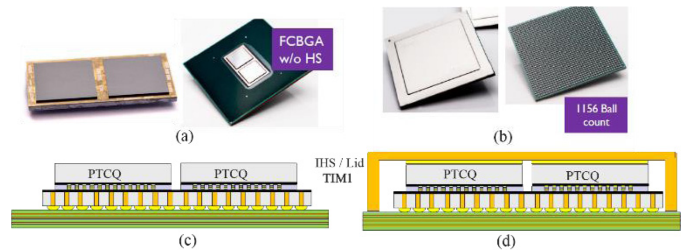

Figure 3. Configurations of 2.5D Si interposer packages with the 8×8 mm^2 thermal test chips: (a) and (c) Bare die (lidless) package; (b) and (d) Lidded package with TIM and lid.

The interposer packages used for the thermal evaluation of the 3D printed impingement coolers are shown in Fig. 3. Two thermal test chips, referred to as PTCQ (Packaging Test Chip version Q [19, 20], are stacked face down on a 20×10 mm^2 Si interposer with a thickness of 100 µm using CuSn µbumps with 40 µm pitch [2]. The interposer contains 10 µm diameter through-Si vias (TSVs) with an aspect ratio of 10. The interposer stacks are packaged in two versions of a 35×35 mm^2 ball grid array package (BGA): lidless packages (Fig.3a, Fig.3c) allowing the cooling solutions to be directly applied to the backside of the chips, and lidded packages (Fig.3b, Fig.3d) that require a TIM between chip and lid. For the lidded packages, a Cu lid with a thickness of 0.3 mm is used. The thermal interface material is a standard silicone based thermal interface material with a specified thermal conductivity of 1.9 W/m-K and a targeted thickness of 80 µm. The schematic of the impingement jet cooling on the lidded package and lidless package are shown in Fig.4. Based on the same architecture design as single die cooling shown in Fig.1, this cooling structure also contains four main parts: inlet plenum, outlet plenum, nozzle plate and impingement cavity, targeted at two PTCQ dies.

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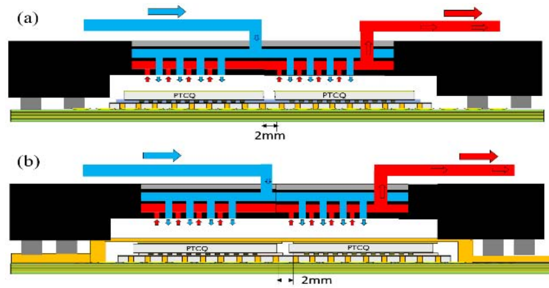

Figure 4. Schematic of 2.5D interposer cooling design concept with lid or lidless package: (a) designed cooler structure for cooling on the bare die; (b) cooler structure for cooling on the lidded package.

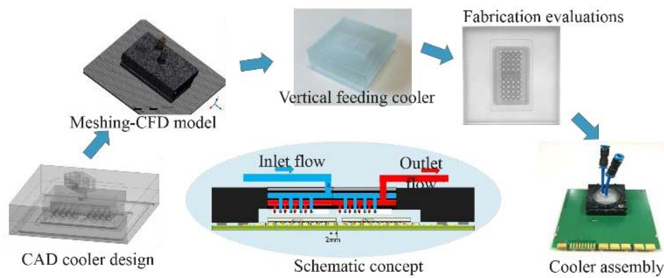

Figure 5. Prototyping flow of 3D printed cooler from concept to the demonstrator.

The prototyping flow for the demonstration of the interposer package cooler for this concept is shown in Fig.5. Based on system requirement such as: flow loop connections, cooler size limitations and assembly constraints, the initial design is proposed. Next, the cooler is designed using the CAD software VariCAD. After that, the CAD file is imported into the ANSYS Fluent modeling software for parameter optimization based on conjugate heat transfer simulations. After several design iterations, the CAD file can be used as input for the 3D printing software platform Fusion 360. After the quality evaluation of the 3D printed cooler, the cooler is assembled on the test board for the thermal performance characterization measurements.

2.1 3D printed cooler design

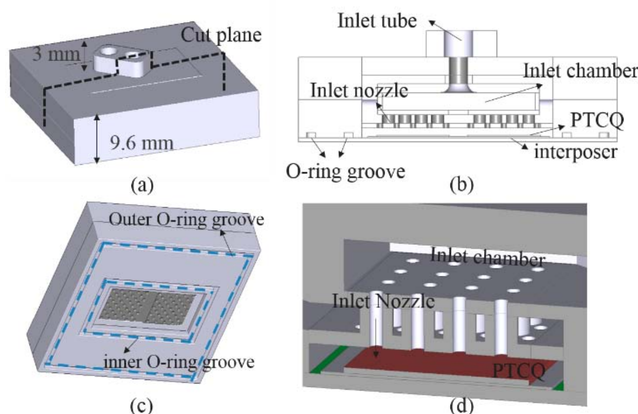

Figure 6. Design structure details of the 3D printed cooler: isometric view (a), cross section view (b) and bottom view (c) of the designed 3D printed cooler; (d) details of the inside nozzle distributed channels.

The cooler has been designed to match the 35×35 mm^2 footprint of the BGA packages and to fit the Si interposer and bonded chips in the cooler cavity. For the cooler design, unit cells of 2×2 mm^2 are used with 600 µm nozzles, resulting in a 4×4 array on inlet nozzles and staggered 5×5 array of outlet nozzles centered on top of each chip. The total cooler size is 35×35×9.6 mm^3 and is connected in the flow loop using 3 mm diameter tube connection structures, shown in Fig.6a. The cross-section view of the internal structure and a bottom view of the cooler are shown in Fig.6b and Fig.6c. A detail of the inlet chamber and the inlet nozzles is shown in Fig.6d. The nozzle plate thickness is 0.5 mm and the cavity height is designed as 1 mm, which is defined as the stand-off height between the laminate and nozzle plate. The dimensions of the groove for the O-ring placement are designed as 0.6 mm depth and 1 mm width. The O-ring is mounted into the groove as shown in Fig.6b and Fig.6c.

2.2 Fabrication of 3D printed cooler

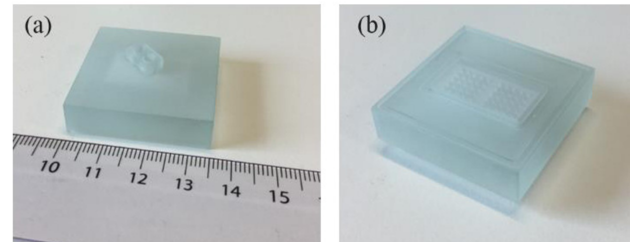

Figure 7. Top view (a) and bottom view (b) of the 3D printed cooler.

The top view and bottom view of the 3D printed cooler for the interposer package are shown in Fig.7, illustrating the inlet/outlet tube connector and the nozzle plate pattern. For the fabrication of the designed cooler, high resolution Stereolithography (SLA) is used with 20 µm layer thickness for the additive manufacturing. The minimal featured size is 70 µm for the XY draw plane and 200 µm for the Z build direction. The tolerance in the X/Y dimension is ±50 µm and ±127 µm. The printing material is a clear ABS-like material (Sonos WaterShed XC 11122), which is resistant to water and humidity. The demonstrator is printed as a whole part by additive manufacturing. For the SLA technology, the cooler is printed layer by layer while the uncured resin is used as supporting materials when the printer moves to the upper level to print the upper layer. The supporting materials (resin) will be removed after all the parts are finished using chemical solvent. Since the 3D printed cooler is printed as a single part, it is difficult to check for internal blockages with residual uncured resin. For this 3D printed cooler, we find that Scanning Acoustic Microscopy technique (SAM) can be used to evaluate the cooler quality [16]. Moreover, in order to increase the structural integrity of the cooler, small support structures between the cavity channel are automatically added by the 3D printing software Fusion 360.

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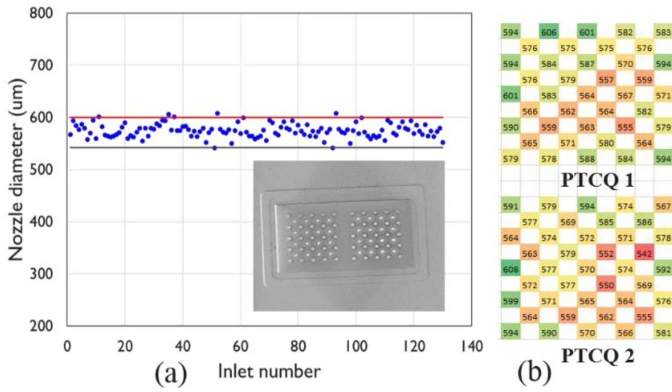

Figure 8. Nozzle diameter evaluations of 3D printed cooler: (a) statistic of nozzle diameters; (b) measured nozzle diameter distribution maps.

All the fabricated inlet and outlet nozzles have been measured in order to assess the fabrication tolerances. Fig.8 shows the measurement data for the nozzle diameters measured from 2 different coolers from the same printing batch. The average nozzle diameter measured for the interposer package coolers is 570 µm, which deviates 5% from the nominal design value of 600 µm for the nozzle diameters. The distribution of the nozzle diameters on the nozzle plate, targeted at the two chips PTCQ1 and PTCQ2 is shown in Fig.8b.

2.3 Assembly of 3D printed cooler

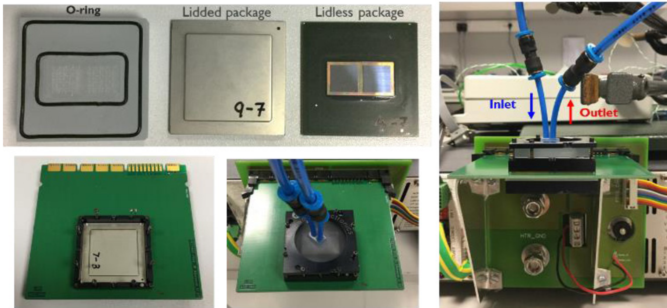

Figure 9. Experimental set up for the 3D printed impingement jet cooler on the 2.5D Si interposer package with lid or lidless in the measurement socket.

The printed cooler is mounted on top of the interposer packages. In case of the lidded package, the cooler is attached on the lid. However, in the case of the lidless package, the cooler is attached on the package substrate, creating a cavity around the Si interposer and bonded chips. In this implementation of the cooler assembly, the liquid coolant will be impinged on top of the chips, but the coolant will also flow in the small gap between the interposer and cooler and between the chips. Therefore, the underfill material is applied between the PTCQ chips and the interposer in order to protect the electrical micro-bumps connections for the bare die package. Fig. 9 shows photographs of the printed cooler, the packages, and the measurement sockets on the test board. O-rings are placed inside the designed grooves on the bottom of the cooler to prevent water leakage issues. Moreover, the O-ring can also act as a buffer for the mechanical assembly of the cooler, especially for large die package to compensate for the potential warpage of the assembly. The assembly of the cooler and package is placed in a measurement socket to perform the thermal measurements. The chip temperature is measured in the diodes of the PTCQ dies.

3. COOLER THERMAL CHARACTERIZATION

3.1 Chip temperature measurements

The assembled cooler is connected to the closed loop thermal/fluid measurement system for accurate flow, pressure and temperature measurements. The flow rate sensor and pressure senor are integrated in the flow loop. For the thermal measurements, the thermal test chip PTCQ can be programmed to generate a full chip power map with 75% area uniformity, referred to a quasi-uniform heating. The full temperature map can be measured with a 32×32 array of diodes across the 8×8 mm^2 area of the chip. The voltage drop across the diode for a constant current is used as the temperature sensitive parameter of the sensor. The 95% confidence interval of the calibrated sensitivity is −1.55±0.02mV/°C for a current of 5µA in the temperature range between 10 and 75°C. The analysis of the propagated measurement uncertainty results in a value of ± 1.8 % for the reported thermal resistance measurements [20]. The overall thermal performance of the cooler is expressed in terms of the thermal resistance R_{th} and the pump power W_p are respectively defined as follows [20]:

$$R_{th} = (T_{avg} - T_{in}) / (Q_{heater}) \quad (1)$$

$$W = \Delta P \cdot \dot{V} \quad (2)$$

where T_{avg} is the measured average chip temperature, T_{in} is the coolant inlet temperature and Q_{heater} is the heat generated in the heater cells based on the measured electrical current and heater voltage. This thermal performance estimation of the assembled cooling solution also includes the heat losses through the cooler material into the ambient and the heat losses through the bottom side of the assembled test board. Moreover, ΔP is defined as the pressure difference between the inlet and outlet nozzle. $\dot{V}$ represents the volumetric flow rate. This thermal performance estimation of the assembled cooling solution also includes the heat losses through the cooler material into the ambient and the heat losses through the bottom side of the assembly, through the test board. The coolant used in this study is DI water while the inlet temperature is set to 10˚C.

As shown in Fig.1b, the nozzle array pattern is a scalable system of repeated unit cells with a single inlet and multiple outlets, under the assumption of identical thermal performance for all unit cells. This includes a constant pressure drop, heat flux and coolant flow rate for each unit cell. The nozzle array of unit cells scales with the chip area. Therefore, the thermal and hydraulic performance metrics can be reported as area independent thermal resistance and pump power to represent the intrinsic thermal and hydraulic behavior. This enables the comparison of the thermal and hydraulic performance of coolers for different chip sizes.

Therefore, the definitions of normalized thermal resistance and normalized pump power are defined as below:

$$R_{th}^* = R_{th} \cdot A \quad (3)$$

$$Wp^* = \Delta P \cdot \dot{V} / A \quad (4)$$

In many applications, the interposer packages combine high power components, such as CPU or GPU, and temperature sensitivity components, such as memory chips, in a single

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package. Therefore, the chip power configuration in this study includes one powered PTCQ die to mimic the "logic" die while the other PTCQ die acts as a "Memory" die without power. In the reported measurement results, the logic die temperature profile will be shown at the left, while the memory temperature profile will be shown at the right hand side.

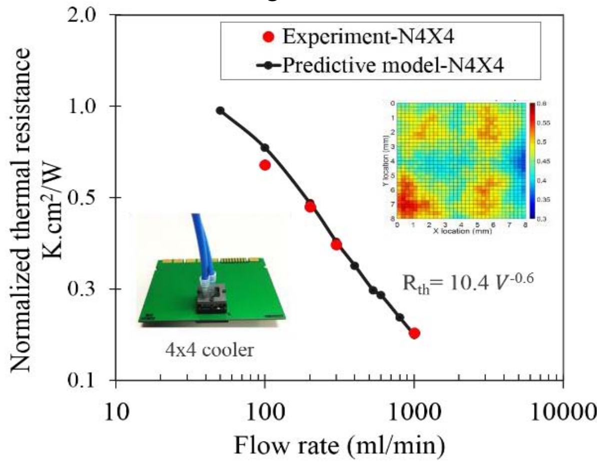

Figure 10. Thermal measurements of bare die liquid jet impingement cooling for a single chip PTCQ package for different coolant flow rates [15].

3.2 Interposer cooling VS single PTCQ die cooling

The impingement cooler mounted to a single chip PTCQ BGA package [15] are summarized as a reference. This cooler contains a 4×4 array of inlet nozzles with 570 µm diameter. The normalized thermal resistance based on the average chip temperature measured in the PTCQ test chip is plotted in Fig.10 for different flow rates. The measured thermal resistance is 0.25 K/W at a flow rate of 1000 ml/min. Using the normalization to express the intrinsic thermal and hydraulic behavior, the normalized thermal resistance is 0.16 cm^2-K/W at a normalized flow rate 0.26 m/s (flow rate=1000 ml/min for a chip area of 64 mm^2) and 0.35 cm^2-K/W at normalized flow rate of 0.08 m/s (flow rate=300ml/min).

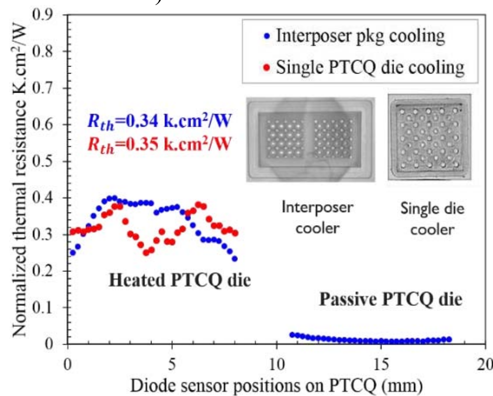

Figure 11. Measured thermal performance comparison between the interposer cooler for the lidless package and single die cooler (logic power=50W; memory power=0W)

The interposer package cooler has been characterized for a power dissipation of 50W in the left chip ("logic") and no power dissipation in the right die ("memory"). The measured temperature profile on both chips is shown in Fig. 11 for the lidless interposer package and compared to the temperature profile of the single chip package for the same normalized flow rate of 0.08 m/s (300 ml/min for the single chip package and 600 ml/min for the interposer package). The results for both coolers show a consistent behavior of the intrinsic cooling performance. This thermal performance can be extrapolated to larger chip area cooling application due to the scalability of the nozzle pattern.

3.3 Cooling on lid vs bare die cooling

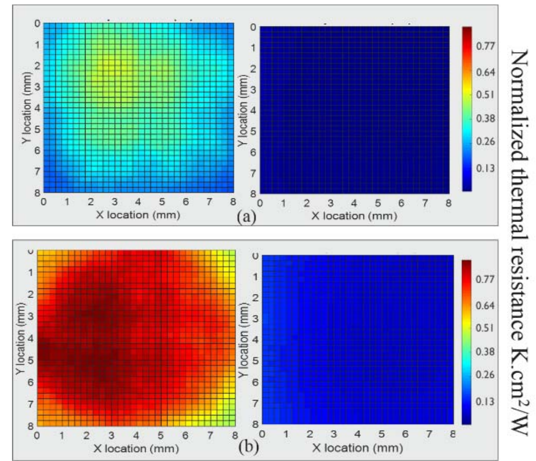

Figure 12. Normalized thermal resistance map measurements (cm^2-K/W) for the 3D printed impingement cooler on the (a) lidless interposer package and (b) the lidded interposer package (Logic power=50 W; memory power=0 W; flow rate =1000 ml/min).

In the next step, the thermal performance of the 3D printed cooler is compared for the lidded and the lidless packages, introduced in Fig. 3. The measured chip temperature distribution maps for both packages are shown in Fig. 12. The temperature profile at the center of the chips is shown in Fig. 13 to allow a more detailed comparison of the thermal behavior. The comparison of the temperature profiles of the two package reveals a significant difference for both the heated chip as well as for the passive chip. The overall thermal resistance of the logic chip is a factor or 2.5 to 3 higher in case of the lidded package compared to the lidless package. This large difference is mainly caused by the presence of the thermal interface material. From the thermal measurements of both packages, the additional thermal resistance of the TIM and lid can be measured as 0.45 cm^2-K/W. Furthermore, it can be observed that the thermal coupling between the logic and the memory die is much higher in the lidded package compared to the lidless package, due to the heat spreading in the Cu lid. As shown in Fig.13, the temperature difference between the lidless and lid package with passive PTCQ die is due to the thermal coupling effects. For the lid package, the thermal coupling is higher due to the existing of the TIM and lid. The thermal path goes along the TIM/lid and also the bottom interposer package.

At a flow rate of 1000 ml/min, the thermal coupling is 4 times higher in the lidded package, compared to the lidless package, as can be seen from Table 1. The thermal coupling effect comes from the temperature increase of the passive die with the heating of active die. Therefore, the thermal coupling is defined as below:

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$$R_{coupling} = \frac{T_{passive-} - T_{in}}{T_{active} - T_{in}}$$

The average thermal coupling is defined as the ratio of the average passive die temperature difference w.r.t. the ambient temperature divided by the average hot die temperature difference w.r.t. the ambient temperature, while the maximum thermal coupling is defined as the maximum passive die temperature difference w.r.t. the ambient divided by the maximum hot die temperature difference w.r.t. the ambient.

Table 1. Thermal coupling at flow rate of 1000ml/min

	Lidded pkg	Lidless pkg
Max. Coupling	21.4%	5.3%
Avg. Coupling	15.4%	3.4%

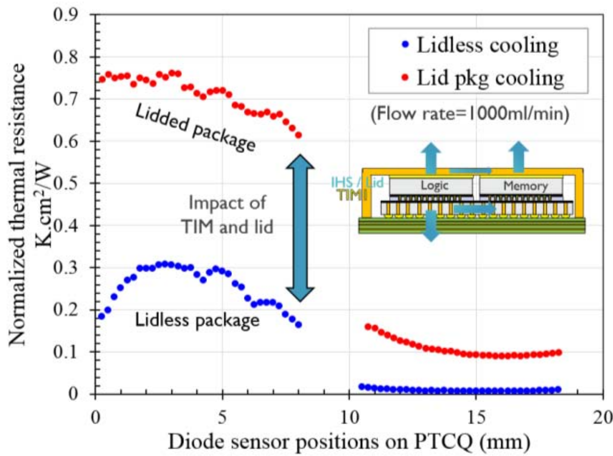

Figure 13. Thermal measurement comparison between the lidless package cooling and lidded package cooling (logic power=50W; memory power=0W; flow rate=1000ml/min).

The measurements results for the lidded and lidless packages are summarized in Table 2 for different flow rates. The presence of the lid (and mainly the TIM) results in a higher chip temperature, where the relative impact of the lid increases as the flow rate increases since the convective thermal resistance decreases with the flow rate.

Table 2. Measured thermal resistance of the lidded and lidless PTCQ packages at different flow rates

Flow rate (ml/min)	Average Thermal resistance (cm^2-K/W)		Maximum Thermal resistance (cm^2-K/W)	
	lidded	lidless	lidded	lidless
300	0.85	0.47	1.11	0.56
400	0.80	0.41	1.14	0.48
600	0.75	0.33	0.91	0.40
1000	0.68	0.26	0.76	0.30

4. PACKAGE LEVEL MODELING AND VALIDATION

The measurement results above show that the presence of the lid and the TIM have a significant impact on the cooling performance of the 3D printed impingement cooler. The beneficial effect of the lid is the improved thermal spreading which results in a decrease of the temperature peak and more uniform chip temperature. The detrimental effect of the lid, is the additional vertical thermal resistance for the heat conduction through the TIM and the lid. A modeling study has been performed to assess this trade-off for the lid for different TIM and lid properties and for different flow rate conditions. First, the modeling approach is introduced. Next, the experimental validation of this approach is presented and finally a design of experiments is performed to assess this trade-off.

4.1 Package-level numerical simulations (FEM / CFD)

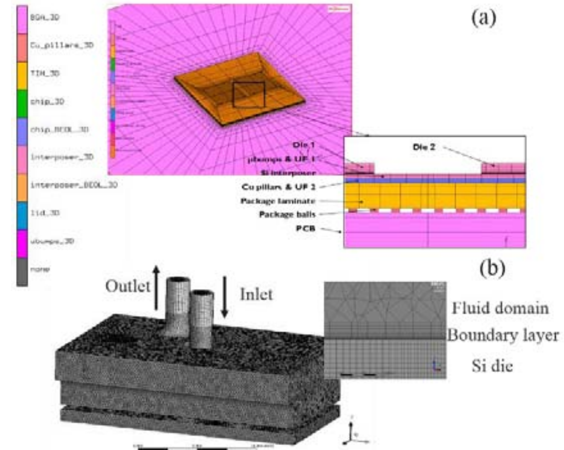

Figure 14. Package model: (a) details of package elements in FE model; (b) mesh of the full cooler level CFD model.

A hybrid modeling approach is used for the thermal analysis of the interposer package coolers to limit the overall simulation time. First, a full conduction-convection model is performed using conjugated heat transfer computational fluid dynamics (CFD) to simulate the heat transfer in the package and the convective heat transfer in the impinging coolant. In order to capture all the heat spreading paths in the structure, not only the lid and TIM, but also the details of the bottom part of the interposer package needs to be included in the model. For the CFD model shown in Fig.14b, a structural mesh with a minimal meshing size of 0.02 mm is used for the solid part, while tetrahedral meshing elements are used for the fluid domain with a meshing size of 0.15 mm. Moreover, the first layer thickness of the boundary layer is 1 µm. The total number of elements in the model is around 5 million. A grid sensitivity study using the Richardson extrapolation resulted in a low truncation error of 0.3 % on the average temperature differences w.r.t. the ambient temperature [20].

In the second step, the heat transfer coefficient distribution on top of the lid is extracted. This distribution is used as a boundary condition input for a conduction model of the complete interposer package using finite element modeling simulations (FEM) in order to perform the DOE for the assessment of the impact of the lid. While changing the properties of the TIM and lid, the assumption is made that the flow distribution and results heat transfer coefficient distribution is not affected. This simplification allows us to focus on the conduction heat transfer in the interposer package and lid using the much faster conduction models. Fig. 14a shows the grid containing 400,000 elements for the finite

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element modeling study including the PCB, the solder balls, the package laminate, the interposer, logic and memory chip, the interconnections between the chips and the package, such as BEOL, micro-bump layer, Cu pillars and underfill. The material properties are listed in Table 3. For the thermal finite element model, the μbumps and Cu pillars arrays embedded in underfill material are replaced by a material with equivalent in plane and out of plane thermal conductivity [18].

The uniform power dissipation is applied as a constant heat flux in the logic die while there is no power in the memory die. The ambient temperature is considered to be at 25ºC. An equivalent convective heat transfer coefficient of 25 W/m^2-K is applied at the bottom of the package to represent the heat transfer from the package towards the PCB. The inlet temperature for the CFD model is set to 10ºC.

Table 3: Material properties used in the thermal simulations

Components	Parameters (mm)	Thermal conductivity (W/m-K)
LID	35×35×0.3	400
TIM	35×35×0.08	1.5 (reduced value to include contact resistance)
Si	8×8×0.2	150
BEOL	8×8×0.01	K_{xy}= 0.2; k_z= 2
μbumps+UF	8×8×0.013	K_{xy}= 0.5; K_z= 4
interposer	20×10×0.1	150
Interposer BEOL	20×10×0.01	K_{xy}= 0.2; Kz= 2
Cu pillars	20×10×0.08	K_{xy}= 0.5; K_z= 8
BGA laminate	35×35×0.3	K_{xy}= 0.8; K_z= 10

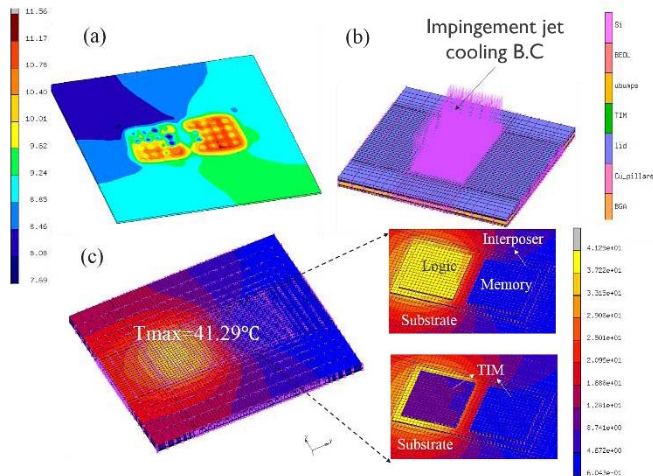

Figure 15. Velocity [m/s] and temperature [°C] modeling results for bare die cooling.

To illustrate the hybrid CFD-FEM approach, Fig.15a shows the heat transfer coefficient extraction results from the full cooler level CFD model. The extracted heat transfer coefficient map is applied on the corresponding lid surface in the FEM model as a convective boundary condition shown in Fig.15b. The temperature map on the lid (left) and die and TIM surface (right) are shown in Fig.15c.

4.2 Model validation studies

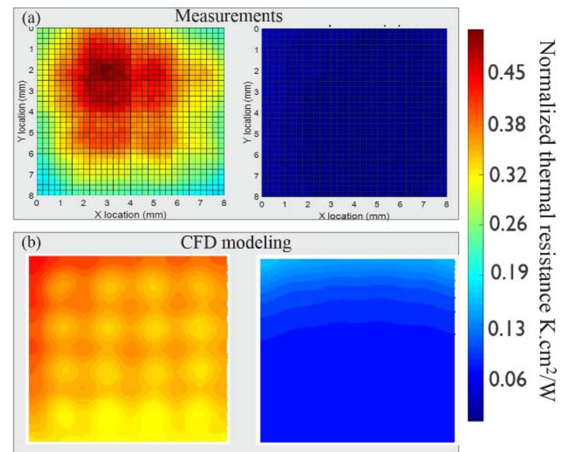

Figure 16. Normalized thermal resistance (cm^2-K/W) distribution comparisons between the measurements and CFD modeling for bare die liquid cooling (logic power=50W; memory power=0W; flow rate = 300 ml/min)

In Fig.16, the thermal resistance distribution maps are compared for the experiments and the CFD model results for the lidless interposer package. The nozzle cooling patterns can be clearly distinguished from the modeled temperature distribution that assumes uniform heat dissipation while the actual PTCQ power map is quasi-uniform with 75% heater uniformity. The measured averaged temperature for the “logic” die based on the bare die cooling at flow rate of 300 ml/min is 0.47 cm^2-K/W while the modeling averaged temperature is 0.46 cm^2-K/W. In general, the full cooler level CFD modeling results agrees well with the measurement data with respect to the average temperature, however differences in local temperature distribution become visible at the location of non-heated parts due to the high heat removal rate. For this level of cooling, more details of the chip power map should be included in order to predict the detailed chip temperature map. Lower temperature around the chip edge in the experiments can be explained due to the absence of the heaters there. The difference between the CFD model and the experimental data for the average chip temperature is 12.6% at a flow rate of 300 ml/min and only 2% at a flow rate of 1000 ml/min.

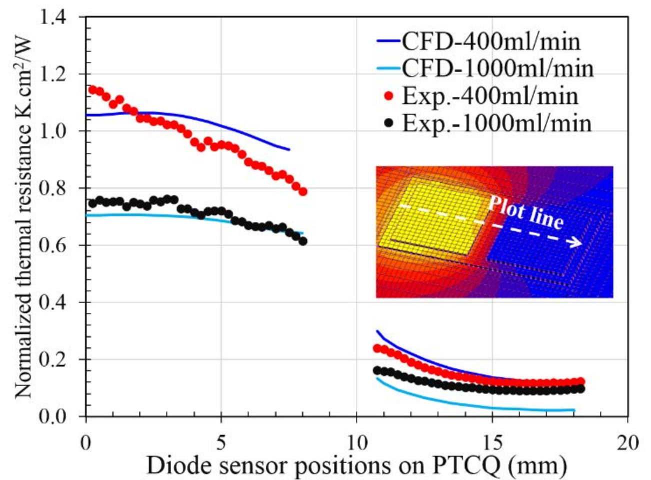

Figure 17. Modeling validation between the hybrid CFD/FEM modeling approach and the experimental results for lidded packages (logic power=50 W; memory power=0 W)

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Fig.17 shows the FE modeling results for the lidded package using the extracted heat transfer coefficient from the CFD models at different flow rates as a boundary condition. The comparison with the experimental PTCQ measurements shows a good agreement for both the active heat chip as well as the passive chip. The relative difference of the normalized thermal resistance (defined as the maximum chip temperature difference w.r.t the ambient temperature) between the hybrid model and the experiments are 7.8% and 4.8% for the flow rates of 400 ml/min and 1000 ml/min respectively. Therefore, the CFD model and FE models for the lidded package cooler are successfully validated and can be used for the extrapolation to assess the impact of the lid.

4.3 Thermal/hydraulic analysis

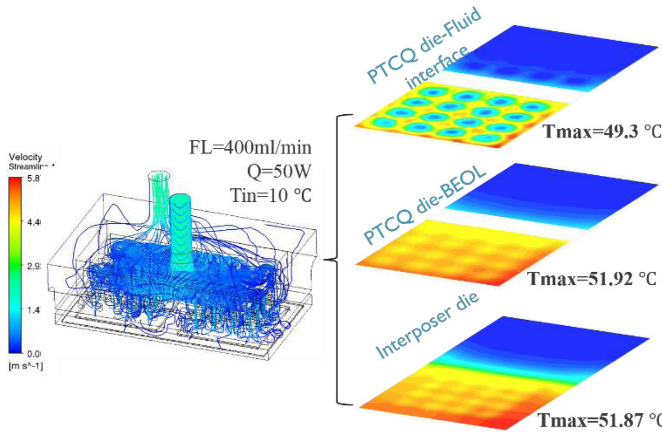

Figure 18. Velocity [m/s] and temperature [°C] modeling results for bare die cooling with different package layers (logic power=50 W; memory power=0 W; flow rate=400ml/min).

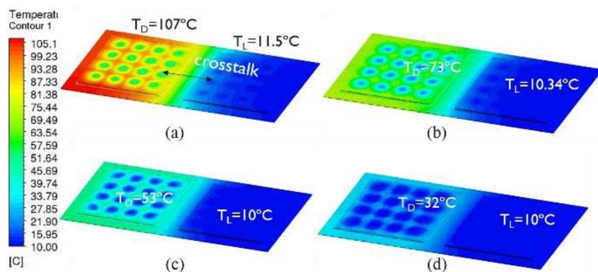

Figure 19. Temperature evolution of bare die cooling under different flow rate for 50W logic power and no memory power: a) FL=100 ml/min; b) FL=200 ml/min; c) FL=400 ml/min; d) FL=1000 ml/min.

Based on the experimentally validated FEM/CFD models, the thermal and hydraulic behavior of the jet cooling can be extracted and analyzed. Fig.18 shows the flow streamlines inside the cooler for the lidless interposer package. It is shown that the high velocity is concentrated in the inlet and outlet tube. The temperature distribution is visualized in different planes of the structure. The footprint of the impinging jets on the temperature distribution is clearly visible on the topside of the die, which is the interface between the solid and liquid domain. The temperature distribution at the level of the heaters in the BEOL and of the interposer help to analyze the thermal coupling. The results show that the thermal cross-talk effects related to the interposer properties are very limited due to the high cooling efficiency of the bare die cooling solution. This thermal coupling between the two chips on the interposer is shown for different flow rates in Fig.19. The thermal cross-talk reduces with increasing flow rate.

5. PARAMETER SENSITIVITY STUDY

The thermal FE model has been used to assess the impact of the lid and TIM properties for the lidded package and to benchmark the results with lidless package for different flow rates. The TIM used for the demonstrator is a standard silicone based TIM, while several high performance TIMs with much lower thermal resistance have been developed [4]. A design of experiments (DOE) has been performed for the thermal conductivity and thickness of TIM and lid layer. The parameters ranges used in the DOE are listed in Table 4. The total DOE includes 625 simulations for each flow rate.

Table 4. Simulation DOE properties for the impact of the lid and TIM.

Parameter	Minimal value	Maximum value
Lid thickness	0.05 mm	1 mm
Lid conductivity	20 W/m-K	600 W/m-K
TIM thickness	0.02 mm	400 mm
TIM conductivity	1 W/m-K	20 W/m-K

The thermal interface material creates a vertical thermal resistance for the heat removal. This thermal resistances scales linearly with the TIM thickness and inverse proportional with the TIM thermal conductivity. The lid at the other hand shows a typical thermal spreading behavior: a thicker lid will result in more later spreading, and thus lower temperature values, but at the same time the vertical thermal conduction resistance increases. Moreover, in case of the lidded package, the cooling is applied on a larger area compared to the lidless package. This trade-off is now illustrated for a high coolant flow rate of 1000 ml/min.

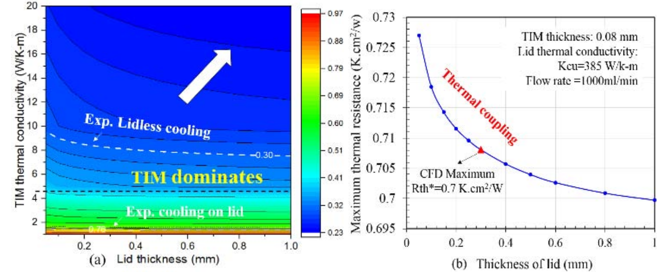

Figure 20. Tradeoff between the lid thickness and TIM thermal conductivity at flow rate of 1000 ml/min (K_{lid}=385 W/m-K; TIM thickness=80 µm).

Fig. 20 shows the analysis for the flow rate of 1000 ml/min for a Cu lid and a TIM thickness of 80 µm. Fig. 20a shows the normalized maximum logic temperature as a function of the TIM thermal conductivity and the lid thickness. It can be seen that the impact of the lid thickness is almost negligible for TIM thermal conductivity values smaller than 4 W/m-K. As the thermal conductivity of the TIM increases, the impact of the lid thickness becomes visible. This behavior is illustrated in Fig.20b for a TIM conductivity of 1.5 W/m-K, where a sharp temperature increase can be observed for lid thickness values below 250 µm. However, due to the high heat removal rate of the impingement cooling on top of the lid, the impact of the lid thickness remains small. The isoline for the value of the lidless

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cooler with maximum thermal performance (0.30 cm^2-K/W) is added in the chart to benchmark the lidless and lidded packages. The measured demonstrator is added as a marker. The comparison shows that a maximum TIM conductivity is 10 W/m-K for a 80 µm thickness (thermal resistance: 8 mm^2-K/W) is required for the lidded package cooling to match the performance of the lidless cooler.

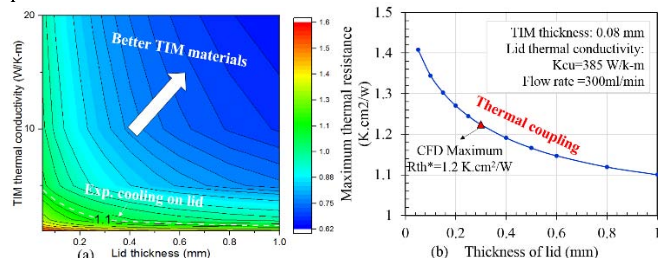

Figure 21. Tradeoff between the lid thickness and TIM thermal conductivity at flow rate of 300 ml/min (Lid thickness=300 µm; TIM thickness=50 µm)

In Fig. 21, the analysis is shown for a flow rate of 300 ml/min, for a Cu lid and a TIM thickness of 80 µm. For this lower flow rate, the spreading effect of the lid is more visible. For TIM conductivity values below 4 W/m-K, the thermal performance remains dominated by the TIM. However, for higher TIM conductivity values, the thermal performance is limited by the reduced thermal spreading in the lid for very thin lid values below 250 µm. Again, the situation of the demonstrator is added as a marker in the chart. For this flow rate, however, the performance of the lidless package (0.56 cm^2-K/W) cannot be reached by the lidded package, even for very low TIM thermal resistance values, due to the dominating effect of the thermal spreading in the lid.

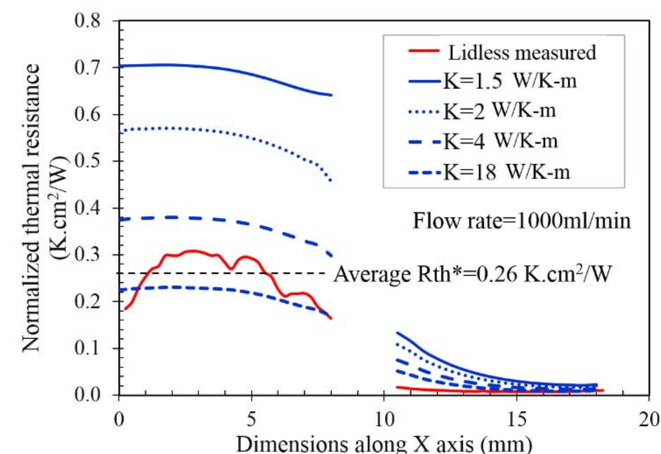

Figure 22. Impact of TIM thermal conductivity on the thermal resistance of the impingement cooler on the lidded package for a flow rate of 1000 ml/min and the benchmarking with the lidless cooling (red curve).

The impact of thermal conductivity TIM on the chip temperature profiles in the interposer package is shown in Fig.22 for a TIM thickness of 80 µm, a lid thickness of 300 µm and a flow rate of 1000 ml/min. The measured profiles for the lidless cooler is added as a reference. This figure shows the temperature profiles for each data point in the chart of Fig. 20a. For higher TIM thermal conductivity values, lower logic temperatures are observed. However, an increased relative thermal coupling is observed for higher TIM thermal conductivity values. This chart shows that, for a TIM with sufficiently high thermal conductivity, the lidded package cooling can achieve the same cooling performance as the lidless package cooling at this high flow rate.

CONCLUSIONS

In this work, we present the design, modeling, fabrication and experimental thermal and hydraulic characterization of 3D-printed impingement coolers applied to 2.5D Si interposer packages. The impingement cooler, matching the size of the 2.5D interposer package with 35×35 mm^2, has been designed with a 4×4 array of inlet nozzles covering each test chip, and with a 5×5 array of outlet nozzles distributed in between. Moreover, the coolers have been fabricated using high resolution stereolithography with the water-resistant Watershed material. The printed nozzle diameters show averaged value of 570 µm and good uniformity. The experimental results of the assembled cooler on the 2.5D interposer package show a good agreement with the package level model CFD/FEM. The simulation results show that the presence of the lid results in a higher, but more uniform chip temperature distribution, where the relative impact of the lid increases as the flow rate increases. An extensive DOE has been performed to assess the trade-off of the lid for different TIMs and flow rate conditions. The parameter sensitivity studies show that with sufficiently low thermal resistance of the TIM (below 10 mm^2-K/W), the lidded package cooling can achieve the same cooling performance as the lidless package cooling at this high flow rate.

Acknowledgments

This work was performed as part of the imec Industrial Affiliation Program on 3D System Integration and has been strongly supported by the imec partners and the imec Reliability, Electrical testing, Modeling and 3D technology teams.

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