Performance and Reliability Study of TGV Interposer in 3D Integration

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Abstract

In this work, a test vehicle of 3D stacking structure using through glass vias (TGVs) interposer as major interconnect has been designed and fabricated. Through the optimum TGV filling process for tapered via, chemical mechanical polishing (CMP) process on heterogeneous materials (glass and copper) and 3D structure assembly process, the test vehicle is successfully built and the measured electrical resistance of TGV shows fair agreement to theoretical value. After that, thermal cycling test is employed to evaluate the reliability of TGVs in the 3D structure. Results show that robust 3D stacking structure with glass interposer has been developed successfully in this study.

1. Introduction

Interposer is one of the most potential solutions for future 3D integration with ultrafine pitch. Silicon interposer has been developed in both industry and academia [1]. However, silicon interposer has limitations, such as low productivity due to limited wafer size, extra expensive semiconductor fabrication processes [2], and poor electrical properties like insert loss and signal crosstalk. On the contrary, glass can be one kind of promising material as interposer because of the excellent properties, such as good electrical resistivity, relatively low CTE compared to organic material [3]-[4], and possible high productivity with big panel size provided by glass suppliers [5].

Recent research studies have mainly focused on three challenges in glass interposer technology: (1) formation of fine pitch via, which is more difficult than through silicon via (TSV) due to the unfavorable etching process [6]; (2) via metallization and via filling process, which become much more complicated because of the rough morphology of TGV surface, and difficulty to fill the tapered via through Damascus electroplating; (3) reliability concern, which is caused by brittleness and poor mechanical strength of glass [7].

For the fabrication process of TGV, two solutions are prevailingly proposed, including blind via electroplating [8] and electroless plating [9]. The blind via method presented by Corning incorporated and ITRI (Industrial Technology Research Institute) contains via formation through laser drilling, via metallization by sputtering and via filling by Damascus electroplating [10]. Electroless plating solution is based on a novel approach utilizing polymer buildup layer on glass, which is put forward by Georgia tech [6]. However, poor adhesive strength between electroless copper [11] and glass could influence the reliability of glass interposer. Besides, Institute of Microlectronics Chinese Academy of Sciences developed a additive method for TGV via filling with inserted tungsten pins enclosed in polymer [12]. Asahi Glass Co., Ltd demonstrates a TGV formation method using conductive paste technology [13]. Dankook University proposed a novel TGV filling method using glass reflow and seedless electroplating process [14]. Nonetheless, these solutions are high cost and not for general use. The electrical performance and thermomechanical reliability analysis based on electroless plating are systematically studied [11], [15], [16]. However, limited works related to glass interposer integration with TGVs is available for the failure mode and reliability analysis.

Concerning the compatibility between TGV and TSV fabrication process, electroplating method is used in our work. This paper develops a 3D stacking vehicle with TGVs interposer. In order to evaluate the reliability of the structure, the electrical resistance is measured before and after thermal cycling test.

2. Test vehicle design

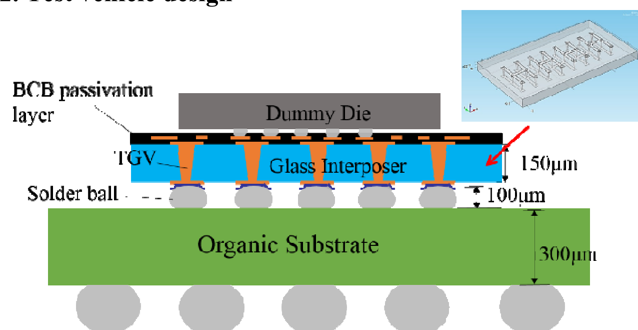

Fig.1 3D stacking structure with glass interposer

As shown in Fig.1, a 3D stacking test vehicle with TGV interposer is designed. A dummy die with Cu-Sn micro-bump will be connected to the glass interposer through Cu-Sn-Cu bonding. The size of glass interposer is 10mm × 10mm × 150μm. The diameter of TGV at the open side is 50μm with 150μm depth, and 300μm pitch. After that, the bonded module will be assembled on designed test substrate through 90μm-diameter solder ball. The Kelvin and Daisy Chain structure patterned on the glass interposer are illustrated in Fig.2.

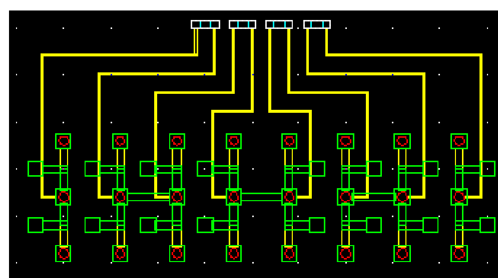

Fig.2 3D stacking test structure pattern

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Corning Borosilicate Glass Pyrex 7740 with 300μm in thickness is selected to form the TGV interposer. Due to the low permittivity, excellent high frequency performance, good chemical and thermal enduring properties, BCB CYCLOTENE 2046-46 is selected as the passivation layer on the surface of glass interposer. Organic substrate with 300μm thickness was chosen as the bottom tier of the 3D stacking structure.

3. Development of 3D integration with glass interposer

3.1 Fabrication of glass interposer

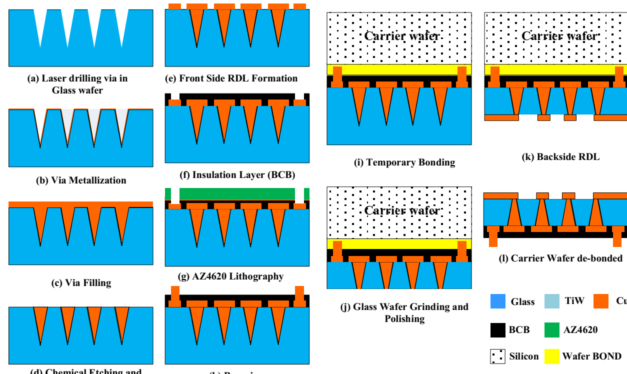

Fig.3 Schematic fabrication process for glass interposer

The schematic fabrication process for glass interposer is shown in Fig.3. The vias are formed directly on glass substrate through laser drill process. After standard clean process, barrier layer TiW (600nm) and seed layer Cu (1μm) are deposited inside vias. With 5% H_2SO_4 and vacuumize pretreatment, the TGV filling results with bottom-up electroplating are displayed in Fig.4. The yield and uniformity of TGV filling could be inspected after HF (49%) erosion. Wet etching and CMP are employed to remove Cu overburden/barrier on the surface of glass wafer.

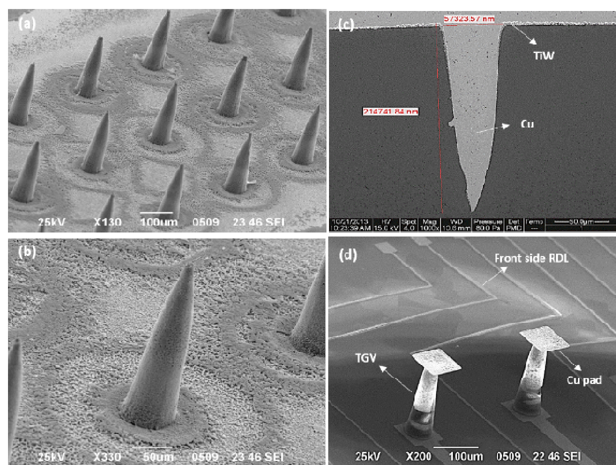

Fig.4 Glass interposer with TGVs fabrication results: (a), (b) TGV filling results after 49% HF etching; (c) Cross-section of TGV filling; (d) 3D view of TGV sample with RDL

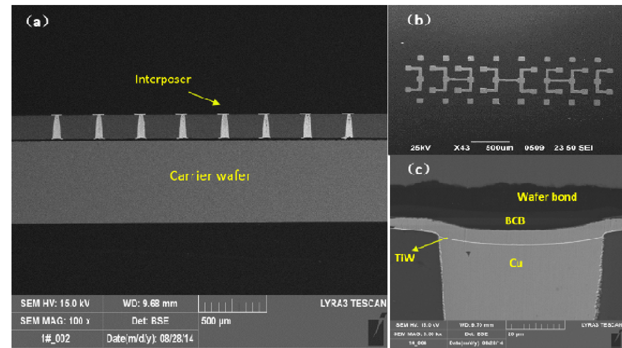

Fig.5 The TGV sample with carrier: (a) Cross section of glass interposer; (b) Pattern of test structure; (c) Passivation layer and temporary bonding layer on TGV

BCB layer used for passivation is realized with good adhesive strength on glass. After that, the glass wafer is temporarily bonded on a carrier wafer. With uniform and void-free temporary bonding quality, the glass wafer is thinned to 150μm until Cu exposure, followed by grinding and CMP. The cross section of glass interposer with upper RDL and bottom bump is shown in Fig.5. The BCB layer with thickness of 8μm and test structure are also shown in Fig.5. Combined the corrosion image and cross section view, a robust glass interposer with TGVs and trace RDL is obtained without electricity open.

3.2 Assembly process of 3D structure

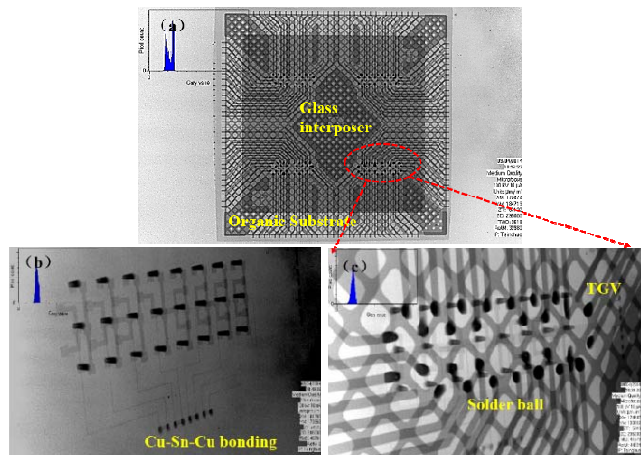

Fig.6 X-ray inspection of 3D assembly results: (a) Top view of assembly results; (b) 3D view of glass interposer bonding, (c) 3D view of assembly structure

Chip-to-chip (C2C) bonding is applied after fabrication of the TGV structure. Pretreatment to Cu surface on the dummy die and Sn surface on glass interposer was done by using 5% H_2SO_4 and Ar plasma, respectively, to remove the oxidation layer on Cu/Sn bumps. In order to prevent the Cu/Sn from oxidizing, the thermo-compression bonding of Cu-Sn-Cu is processed under Formic acid ambience.

Different bonding pressure and bonding time with peak bonding temperature of 260℃ are investigated systematically to reduce the warpage caused by CTE mismatch during and after thermo-compression bonding and ensure good bonding quality and intermetallic compound (IMC) formation. Results indicate that the low bonding time and high bonding pressure

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can realize good connectivity with low warpage. The optimum bonding force is 500g with a dwell time of 20sec. Fig.6 shows the X-ray detection of glass interposer bonding module. The bonded module is assembled on organic substrate through solder ball mount and reflow process, which exhibits a good connectivity between the three tiers. The prototype of 3D stacking structure and glass interposer chip are exhibited in Fig.7.

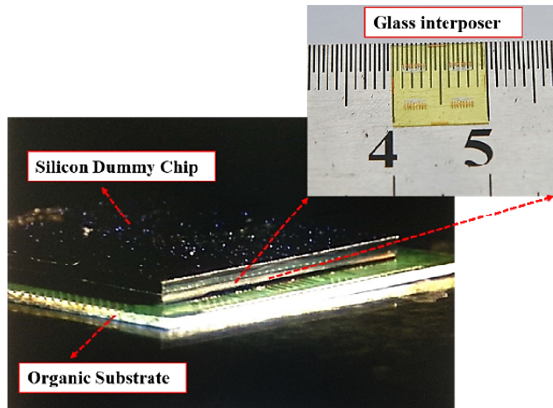

Fig.7 Prototype sample and single glass interposer chip

However, the risks existing in TGV fabrication and assembly process should be concerned carefully. For TSV in silicon, crack failures occur mainly along the crystallographic planes [4]. However, for TGV in glass, crack propagation can be divided into three categories: radial crack, circumferential crack and interfacial crack [17]. Existence of TGVs decreases the inherent strengthen of glass. Cracks are initiated result from glass surface defects since glass is amorphous material. Therefore, the source of crack in glass should be investigated in details. First of all, the cracks generated from laser drilling will propagate in the following fabrication and assembly process. Secondly, the CMP and thinning process of glass could generate great shear stress leading to cracks. Moreover, glass interposer with 300μm thickness is prone to warp during high temperature. High stress and nonuniformity pattern would bring warpage of glass interposer. Fig.8 illustrates the crack after CMP process with top view and cross section. These cracks could propagate in the following process and finally lead to failure of TGV. In order to eliminate the high stress during CMP and thinning, alternative methods should be investigated to remove the Cu overburden without damage.

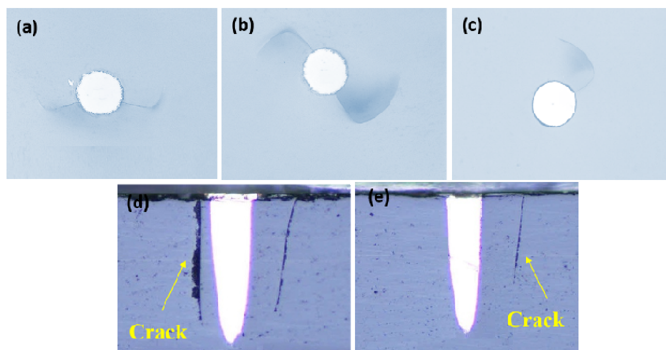

Fig.8 Crack after CMP: (a), (b), (c) Top view of crack around TGV; (d), (e) Cross section of crack

4. Results and discussions

4.1 Electrical characterization of TGV

The resistance of one single TGV is measured in the case of 3D stacking structure by four point Kelvin structure. During I-R Kelvin model test, the current scans from 1mA to 100mA with increasing step of 1mA. Fig.9 shows the plot of single TGV resistance distribution obtained by measuring ten sets of Kelvin structures. By means of this method, the resistance of single TGV could exclude the resistance accumulation from metal trace and micro joint [18]. Finally, the mean value of ten resistances are calculated as 9.11mΩ, which is higher than theoretical value 3.25mΩ.

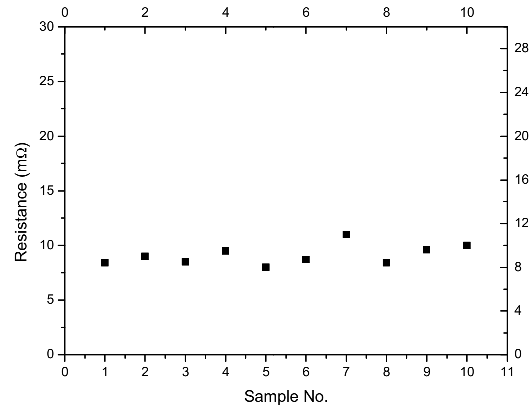

Fig.9 Tested resistance of one single TGV by Kelvin structure

The reasons for this deviation are analyzed in detail. Firstly, the inaccuracy of the Cu resistivity could result in high resistance. The normal resistivity of copper $1.7\times10^{-8}\Omega\cdot m$ is applied in the TGV resistance theory calculation, which may be not accurate for electroplated copper. Secondly, the copper surface oxidation during the fabrication process could increase the interface resistance. Thirdly, the voids or seams inside TGV could highly influence the resistance through diminishing the cross-section area of TGV. Moreover, the resistance of the thin film barrier layer TiW with thickness of 200nm was ignored in this calculation, which could generate higher resistance. Some other contact resistance between the interface are also discarded during calculation.

4.2 Reliability study

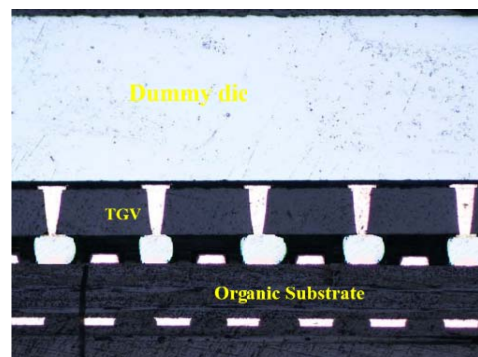

Fig.10 Cross-section of 3D stacking structure after TCT

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In order to evaluate the reliability of the 3D stacking structure, thermal cycling test (TCT) is performed. Refer to JEDEC standards (JESD22-A104 condition B), samples are placed in the test chamber setting temperature ranging from -55℃ to +125℃ with 3 cycles per hour for 500 cycles. Fig.10 shows the cross section of 3D stacking structure after TCT. The solder balls contact the TGVs and Cu pad on organic substrate with good connectivity. No reliability issue is found from the cross section of 3D stacking structure. Table.1 shows the mean resistance measurement at different readout points before and after TCT. The mean resistance after TCT reaches to 9.97mΩ with slight changes from the initial value.

Table.1 Electrical measurement of TGV

Resistance	Initial Value (mΩ)	Value after TCT (mΩ)
Mean value	9.11	9.97

5. Conclusions

In this work, a 3D stacking structure with TGV interposer is designed and fabricated. With appropriate TGV electroplating parameters, CMP and assembly process, the resistances of single TGV are tested through Kelvin structure, which show good agreement with theoretical resistance. After the thermal cycling test, the electrical and reliability performance of 3D stacking structure have been evaluated and analyzed. The results show that the 3D stacking structure with glass interposer has been successfully fabricated with good reliability.

Acknowledgments

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