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Optimization and Evaluation of Sputtering Barrier/Seed Layer in Through Silicon Via for 3-D Integration

Tiwei Wei, Jian Cai*, Qian Wang, Yang Hu, Lu Wang, Ziyu Liu, and Zijian Wu

Abstract: The barrier/seed layer is a key issue in Through Silicon Via (TSV) technology for 3-D integration. Sputtering is an important deposition method for via metallization in semiconductor process. However, due to the limitation of sputtering and a "scallop" profile inside vias, poor step coverage of the barrier/seed layer always occurs in the via metallization process. In this paper, the effects of several sputter parameters (DC power, Ar pressure, deposition time, and substrate temperature) on thin film coverage for TSV applications are investigated. Robust TSVs with aspect ratio 5∶1 were obtained with optimized magnetron sputter parameters. In addition, the influences of different sputter parameters are compared and the conclusion could be used as a guideline to select appropriate parameter sets.

Key words: barrier/seed layer; Through Silicon Via (TSV); sputtering; optimization

1 Introduction

Three-dimensional (3-D) integration is a major trend in the future of semiconductor. As the core vertical interconnection, Through Silicon Via (TSV) has drawn lots of attention in 3-D integration. TSV offers numerous significant advantages, such as high density interconnection, high performance, low power consumption, and multifunctionality, to name a few[1,2].

The key processes for through silicon via include via formation, isolation, metallization, and filling[3]. Several approaches are employed during barrier and seed layer deposition for metallization, such as Chemical Vapor Deposition (CVD), Physical Vapor Deposition (PVD), and Atomic Layer Deposition (ALD). There are many reasons PVD magnetron sputtering is widely used for the barrier/seed layers deposition of TSV. Firstly, sputtering can be used to deposit metals with different melting points. Secondly, deposition of alloys, such as TiW, can be accomplished. Thirdly, it is economical at a high deposition rate. And last but not the least, the purity of sputtered films is superior[4]. However, poor step coverage of the deposited film layer always occurs when the TSV aspect ratio is increased by magnetron sputtering. Lühn et al.[5] from IMEC investigated the deposition limit with conventional sputtering process, which showed an Aspect Ratio (AR) of 2.5∶1.

The step coverage of the film deposited on the sidewall of TSV plays a crucial role in the whole TSV fabrication process, especially in the via filling process. Furthermore, discontinuous film would influence the reliability of devices and capacitance characteristics of RLC circuits due to copper-to-silicon diffusion. Figure 1 shows a sketch of via filling results with continuous and discontinuous barrier/seed layer. The plating system used in this paper combines conformal and bottom-up filling mechanisms, which has been described in previous publications[6]. As shown in Fig. 1, four additives (suppressor, accelerator, chloride ions, and leveler)

• Tiwei Wei, Qian Wang, Yang Hu, Lu Wang, Ziyu Liu, and Zijian Wu are with the Institute of Microelectronics, Tsinghua University, Beijing 100084, China. E-mail: williamwei129@mail.tsinghua.edu.cn.
• Jian Cai is with both the Institute of Microelectronics and Tsinghua National Laboratory for Information Science and Technology, Tsinghua University, Beijing 100084, China. E-mail: jamescai@tsinghua.edu.cn.
* To whom correspondence should be addressed.
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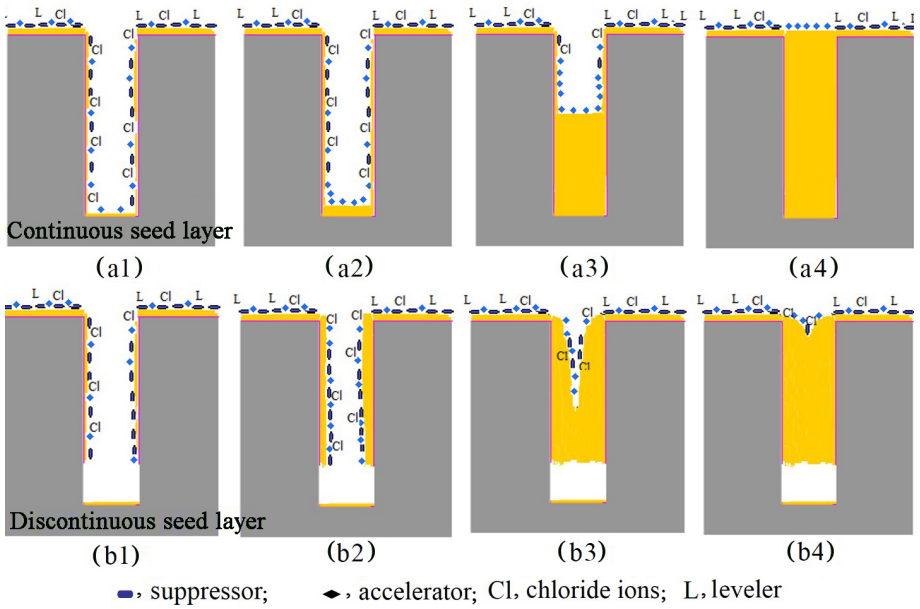

Fig. 1 Via filling results: (a) TSV with continuous barrier/seed layer; (b) TSV with discontinuous barrier/seed layer.

with different concentrations were mixed with the basic copper plating solution. Normally, the accelerators are applied as precursors and form an adsorption complex layer to improve the electron transport[7]. When a wafer surface is adsorbed with suppressor, this can inhibit copper deposition. The additive leveler can eliminate the deposition on the surface and top of the via[8]. However, the electrical conductivity is poor at the bottom of the via owing to the discontinuous barrier/seed layer shown in Fig. 1b. Here, the copper inside the via will grow conformally with voids at the bottom.

Different approaches have been developed to solve the problem. The first approach includes geometrical filtering of sputtered flux and increasing the surface mobility of deposited atoms on the wafer surface[9]. Golovato et al.[10] used a rectangular scanning geometry with collimated PVD system, which eliminated the wafer center-to-edge variations. This system could be used for TSV barrier/seed layer deposition with an aspect ratios of 5∶1 and above. However, this method showed low efficiency and low deposition rate in accordance with the aspect ratio of collimator holes. Carazzetti et al.[11] developed a PVD system by modifying a long-throw process chamber, where TSVs with aspect ratios from 4∶1 to 8∶1 exhibited a bottom coverage of 4% to 1%. Furthermore, the surface mobility of deposited atoms on the wafer surface was increased by thermal reflow, so that atoms could migrate down into deep cavities. Nevertheless, all of the above methods suffer from poor efficiency and high cost. Another method used in-flight ionization of sputtered flux to extend PVD, this technology can also improve the uniformity of the film layer. Weichart and Elghazzali[12] developed a High Power Impulse Magnetron Sputtering (HIPIMS) technology on rotating PVD magnetron sources for Ti/Cu deposition in TSV. The continuous layers inside vias achieved AR of 10∶1. However, this solution is uneconomical. What's more, the barrier and seed layer can be enhanced by electroless deposition and electroplating repair. Inoue et al.[13] and Cho et al.[14] showed that an electroless plating process can improve the continuity of the seed layer effectively. Shen et al.[15] proposed a seed layer repair process using an electroplating method, which can repair the discontinuous copper seed layer at the bottom of TSV with a diameter of 20 μm and depth of 70 μm. Although a continuous seed layer inside TSV can be achieved using the above technology, it is worthwhile investigating conventional PVD magnetron sputtering because of its low cost.

In this paper, we chose TiW/Cu as the barrier/seed layer as they are widely used in TSV fabrication. Systematic experiments were conducted to evaluate the effects of key process parameters (deposition time, Ar pressure, DC power, and substrate temperature) on TiW/Cu coverage through conventional PVD sputtering. During the discussions in Section 4, the deposition rate and film continuity of TiW/Cu were

investigated in detail to evaluate effects of the process parameters mentioned above. Finally, optimization rules for parameter selection were given for TiW/Cu deposition, which could be verified through the TSV filling result with an aspect ratio of 5∶1.

2 Principles of Magnetron Sputtering

Figure 2 shows a schematic diagram of magnetron sputtering deposition. As shown in the diagram, the ever present "free electrons" will immediately be accelerated away from the cathode when the high voltage turns on. These accelerated electrons will drive the outer shell electrons off the neutral gas atoms (Ar), and leave a positively charged "ion" (Ar^+). In the mean time, the positively charged ions (Ar^+) are accelerated into the cathode, strike the target surface with more free electrons, and exchange metal atoms from the target where magnets are designed to trap the free electrons in a magnetic filed. The metal particles (TiW/Cu) are then deposited onto the surface of the wafer.

The mean free path of sputtered metal particles has a close relationship with argon pressure, which is expressed as[14]

$$\bar{\lambda} = \left[\sqrt{1+\frac{m}{40}}\pi\,(r+r_{\mathrm{Ar}})^2\,n_{\mathrm{Ar}}\right]^{-1} \tag{1}$$

where $\bar{\lambda}$ is the mean free path of the sputtered metal particle, n_{Ar} is the molecular density of argon, m is the relative atomic mass of the sputtered particle, r and r_{Ar} represent the atomic radius of the sputtered particle and argon, respectively.

S_c is the sticking coefficient , which is given below:

$$S_c = f(\theta)\mathrm{e}^{\frac{-E_a}{kt}} \tag{2}$$

The coefficient is a function of surface temperature t, surface coverage, and structural details k as well as the kinetic energy of the sputtered particle E_a.

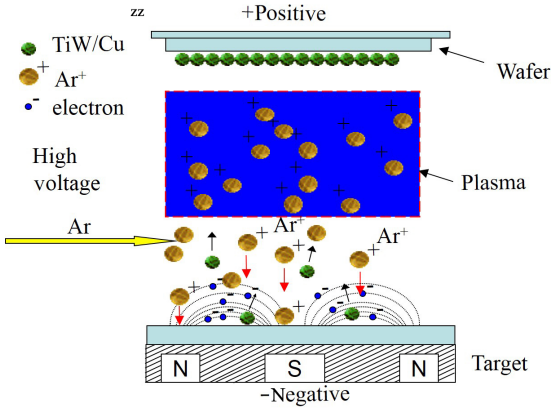

Fig. 2 Magnetron sputtering process schematic diagram.

According to the principle of magnetron sputtering deposition, factors such as Ar pressure and substrate temperature will be discussed to improve the step coverage of TiW/Cu with different aspect ratio TSVs.

3 Experimental Details

3.1 Wafer preparation

A normal via formation process was used for wafer preparation. Photoresist was coated on the 4-inch silicon wafer and patterned with feature opening. Next O_2 plasma treatment was used to remove the extra photoresist. Deep Reactive Ion Etching (DRIE) was used for blind via fabrication. A standard cleaning process was used to remove the inorganic impurities, which can increase the surface sticking coefficient. In addition, a 500-nm silicon oxide was deposited by thermal oxidation as an insulation layer. Experiments were conducted with magnetron sputtering equipment.

3.2 Evaluation of film coverage inside via

To evaluate the film coverage of TSV, wafers with vias were cleaved and analyzed by cross-section, followed by Scanning Electron Microscope (SEM), Focused Ion Beam (FIB), and Energy Dispersive X-Ray Analysis (EDAX). The continuity of TiW/Cu inside the via was checked with Back Scattered Electron imaging (BSE) mode in SEM. Different positions of the sidewall inside via were measured to characterize the step coverage.

As shown in Fig. 3, film is disproportionately deposited at the top corners, and coverage is poor at the bottom corners of the via because of the geometrical shadowing[15]. Voids and seams in copper filled TSV are likely to be produced due to the poor step coverage at the bottom corners. The "overhang" at the top corners of the via will also cause problems during electroplating, and is the result of an over deposited TiW/Cu layer.

In Fig. 3, different positions from point 1 to point 17 along the side of via are chosen to evaluate the step coverage of TSV. Where W is the diameter of TSV, H is the depth of TSV, T_{t} represents the film thickness on the wafer surface, and T_{c} shows the film thickness on the top corner of the via. T_{b} stands for the film thickness at the via's bottom center, T_{m} represents the thickness at the middle of the sidewall, and T_{s} is the film thickness at the via's bottom corner, which has a high impact on the uniformity of current density in the TSV filling process. Film thickness inside TSV is difficult to measure, especially in the bottom corner, so T_{m} and T_{b}

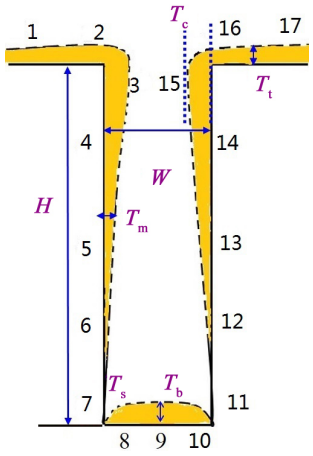

Fig. 3 Measurement of positions and film continuity definitions.

are chosen to evaluate the continuity and step coverage of TSV.

3.3 Design of Experiment (DOE) for magnetron sputtering

The DOE for sputtering films is shown in Table 1. An initial vacuum pressure of 0.006 mTorr is achieved using a turbomolecular pump backed by a mechanical pump. A pre-sputtering clean solution using Ar plasma is essential before film deposition. The normal substrate temperature is 20 ℃, and the substrate is mounted on the sample holder located at a distance of about 125 mm from the cathode. The total gas flows are controlled at 17.3, 23.13, 34.4, 34.57, 41.05 sccm, which correspond to the Ar pressure of 4, 5, 6, 7, 8 mTorr. To evaluate the influence of DC power on magnetron sputtering, five DC powers of 250, 300, 350, 400, and 450 W are used. The rotation mode is used during sputtering, which can provide a more uniform and conformal coating inside a TSV oriented in different directions.

Table 1 DOE for TiW/Cu sputtering.

Item	DT/s	P/W	AP/mTorr	t/℃
N1	2000/1666	300/250	4/5	20
N2	4000/2777	300/250	4/5	20
N3	2000/1666	300/250	6/7	20
N4	2000/1666	300/250	5/4	20
N5	2000/1666	300/250	8/8	20
N6	2000/1666	350/300	4/5	20
N7	2000/1666	400/350	4/5	20
N8	2000/1666	450/450	4/5	20
N9	2000/1666	300/250	4/5	300

Notes: DT, deposition time; P, DC power; AP, argon pressure; t, substrate temperature; 1 mTorr = 133.3 Pa.

4 Results and Discussion

4.1 Barrier/seed layer coverage with baseline parameters

To illustrate the full step coverage inside TSV, 17 testing points are chosen along its sidewall. Figure 4 shows the thickness of TiW/Cu of 30-μm and 50-μm TSVs with aspect ratios of 5∶1 and 3.6∶1, respectively. As shown in Fig. 4a, the Cu thickness at the bottom is 11.7 nm, and 29.5 nm at the middle sidewall, but the thickness at the bottom edge is less than 8 nm. The seed layer along the middle sidewall and the bottom edge is discontinuous. Figure 4b shows that the Cu thickness at the bottom is 21.6 nm, the thickness of the middle sidewall is 32.2 nm, and the thickness at bottom edge is also very thin and discontinuous. As expected, the film thickness is the thinnest at the bottom corner inside

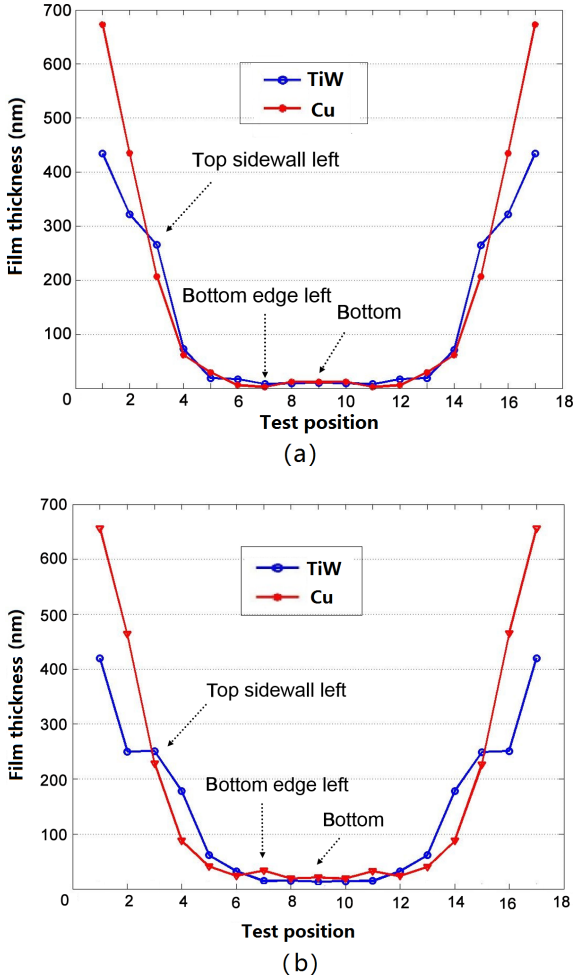

Fig. 4 The thickness of TiW/Cu with baseline parameters at different test positions: (a) 30-μm TSV with an aspect ratio of 5∶1; (b) 50-μm TSV with an aspect ratio of 3.6∶1.

the via because of the geometrical shadowing. The film thickness begins to decrease sharply at the top corner of the via since the TiW/Cu atoms are difficult to deposit on the sidewall. Comparing the two deposition profiles shown in Fig. 4, the film continuity of 50-μm TSV with AR = 3.6∶1 is better than that of 30-μm TSV with AR = 5∶1. Nevertheless, the TiW/Cu layer is still discontinuous using the baseline sputter parameters that can be seen clearly from SEM observation shown in Fig. 5.

As shown in Fig. 5, the scallop-like shapes consist of many micro-concaves deriving from the repetition of isotropic Si etching and passivating layer deposition in the Bosch process. The seed layers along the sidewall inside the via are thin and discontinuous, because the deposited atoms could not reach the upper regions of concaves easily without sufficient power and Ar pressure.

4.2 Effect of the deposition time on film coverage

In order to investigate the variation of film coverage with increasing of film thickness, different deposition times are tested. The deposition time of TiW is increased from 2000 s to 4000 s, and the deposition time of Cu raised from 1666 s to 2777 s. As shown in Fig. 6, the continuous TiW/Cu along the sidewall was achieved by increasing deposition time. For a 50-μm TSV with an aspect ratio of 3.6∶1, the thickness of barrier/seed layer in the middle sidewall is 113.2 nm/111.7 nm. The thickness of the barrier and seed layer at the bottom was also improved, reaching 21.9 nm/27.7 nm. Similarly, the film thickness in the middle sidewall for 30-μm TSV with an aspect ratio of 5∶1 achieved 43.7 nm/40.9 nm. Overall, the barrier/seed layer coverage was sufficient for the subsequent electroplating.

However, this method results in an expensive manufacturing process because of the longer deposition time and higher cost of consumables[16]. In addition, thick TiW/Cu can cause overhang at the top corner of the via especially for a small diameter TSV, as shown in Fig. 7[17].

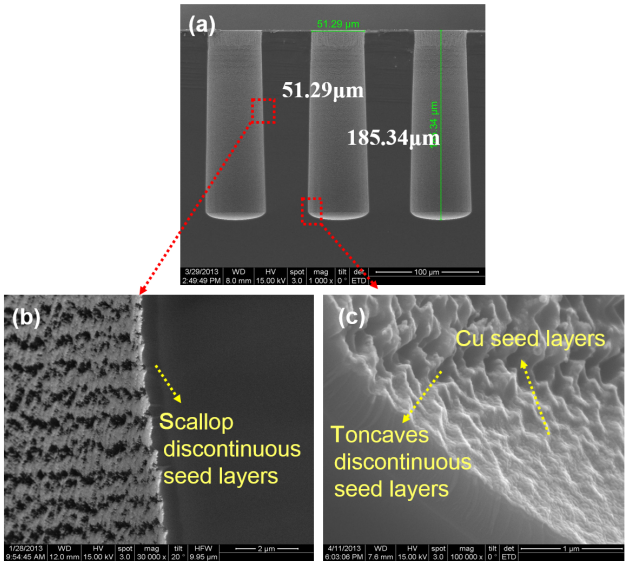

Fig. 5 Scallop-like shapes inside 50-μm TSV with an aspect ratio 3.6∶1: (a) TSV after TiW/Cu deposition; (b) Scallop with discontinuous seed layers; (c) Concave inside the bottom of TSV.

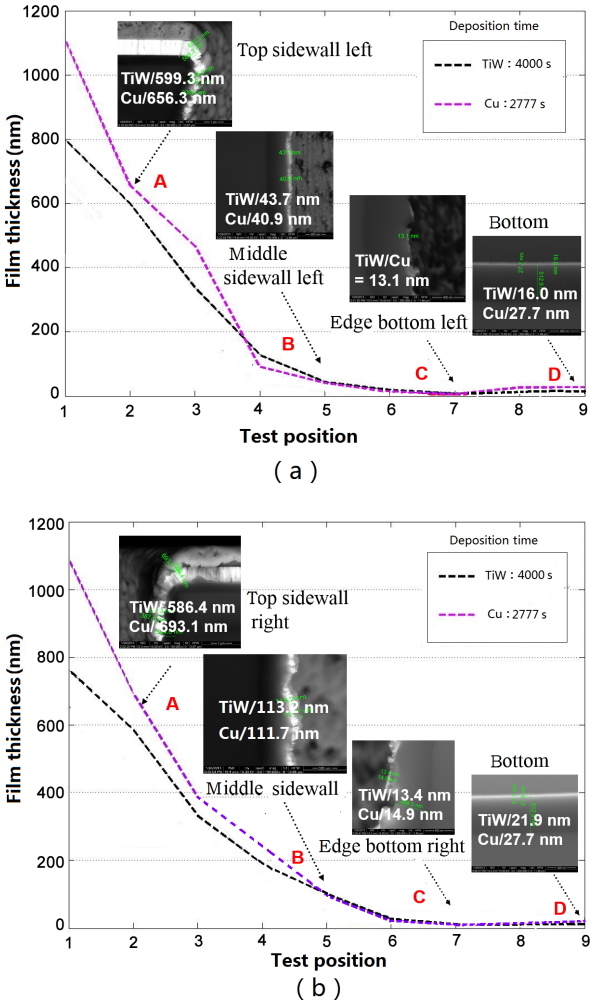

Fig. 6 Variation of the TiW/Cu thickness by increasing deposition time: (a) 30-μm TSV with an aspect ratio of 5∶1 and (b) 50-μm TSV with an aspect ratio of 3.6∶1.

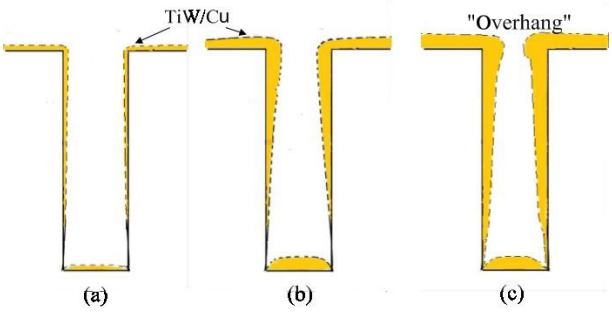

Fig. 7 Overhang at the top corner of via with increasing deposition time.

4.3 Effect of argon pressure on film coverage

The TiW/Cu thicknesses measured by SEM-BSE with different argon pressures are shown in Fig. 8. For all argon pressures, the DC power and substrate temperature are maintained with baseline parameters. As shown in Fig. 8, continuous films are achieved by increasing argon pressure.

Figure 9 illustrates the deposition rate of TiW and Cu versus the changes in argon pressure. The deposition rate of Cu increases from 0.3673 nm/s at 4 mTorr to the maximum of 0.3936 nm/s at 5 mTorr, and then decreases with the ascent in argon pressure to 0.3323 nm/s at 8 mTorr. The deposition rate of TiW monotonically increases from 0.2098 nm/s to 0.2477 nm/s as the argon pressure increases from 4 mTorr to 8 mTorr, but deposition rate does not have a linear relationship

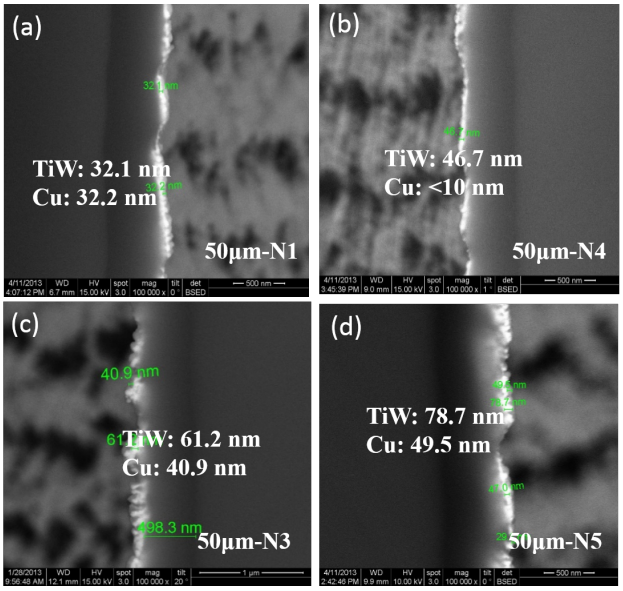

Fig. 8 Mid-sidewall TiW/Cu thickness of 50-μm TSV with different argon pressures: (a) 4 mTorr/5 mTorr; (b) 5 mTorr/4 mTorr; (c) 6 mTorr/7 mTorr; (d) 8 mTorr/8 mTorr.

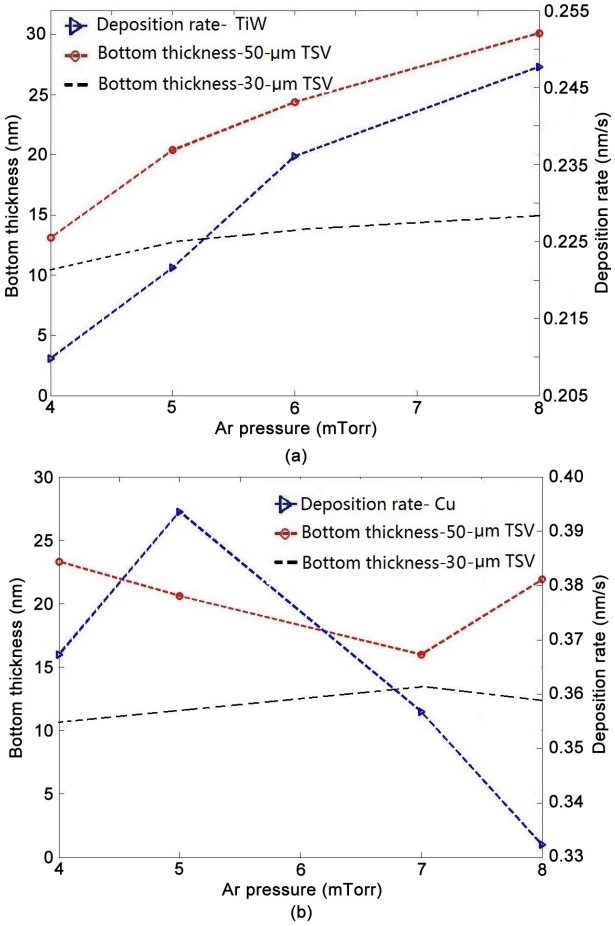

Fig. 9 Effects of Ar pressure on the deposition rate and bottom film thickness: (a) TiW variation curve and (b) Cu variation curve.

with argon pressure. As the pressure increases, the deposition rate rises initially, followed by a slower rate between 6 mTorr and 8 mTorr. Moreover, the glow discharge no longer occurs as the argon pressure is below 3.5 mTorr.

As the argon pressure is set at a lower level, the mean free path of the sputtered particle will increase as shown in Eq. (1), in turn the sputtered atoms have enough kinetic energy to easily deposit them onto the wafer surface. Insufficient argon ions in the chamber lead to low deposition rates at the first stage. With the increase of argon pressure, more gas molecules are admitted to the chamber and dissociated to exchange the TiW/Cu atoms from the target with high energy. High deposition rates are obtained as a result of the high energy particles. Nevertheless, the deposition rate decreases as the argon pressure exceeds a specific value. Significant energy loss from the exchanged metal particles results from collisions between the redundant

gas molecules, therefore reducing the deposition rate.

The effects of argon pressure on film thickness at the bottom inside of TSV are also presented in Fig. 9. For 50-μm TSV with an aspect ratio of 3.6∶1, the bottom film thickness increases with the rise in deposition rate. The increase of TiW/Cu bottom thickness is not obvious for 30-μm TSV, because via depth is so high that the deposition atoms could not easily reach the via bottom. Combining results from Figs. 8 and 9, the optimal argon pressure for TiW/Cu deposition is 8 mTorr/5 mTorr.

4.4 Effect of DC power on film coverage

Figure 10 shows how the barrier/seed layer thickness at the midpoint inside TSV varies with the increase of DC power. It was found that increasing DC power improves the film thickness and continuity of barrier/seed layer. The sputtered atoms arrived at the upper concave regions through large kinetic energy gained from the high DC power. The effect of DC power is more obvious than argon pressure. Good continuity was achieved with the experimental parameters N8, which are 450 W/450 W for TiW/Cu sputtering.

Figure 11 illustrates the deposition rate and bottom thickness inside TSV versus the DC power. Compared to argon pressure, DC power has a more significant influence on deposition rate. The deposition rate of TiW/Cu increases sharply with the rising of DC power, and the bottom thickness inside TSV increases steadily. As the DC power dissociates argon molecules

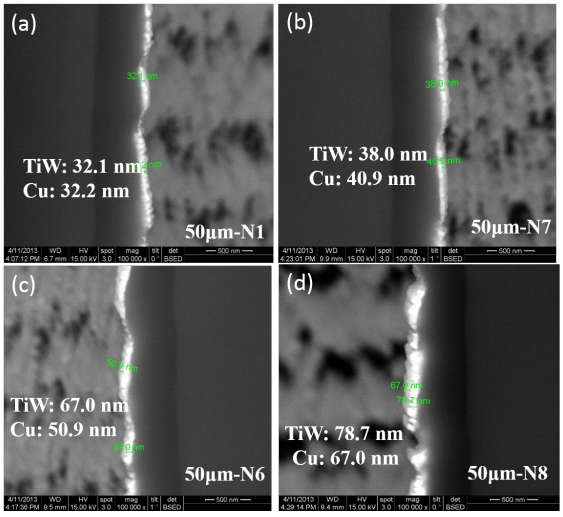

Fig. 10 Mid-sidewall TiW/Cu thickness of 50-μm TSV with different DC powers: (a) 300 W/250 W; (b) 400 W/350 W; (c) 350 W/300 W; (d) 450 W/450 W.

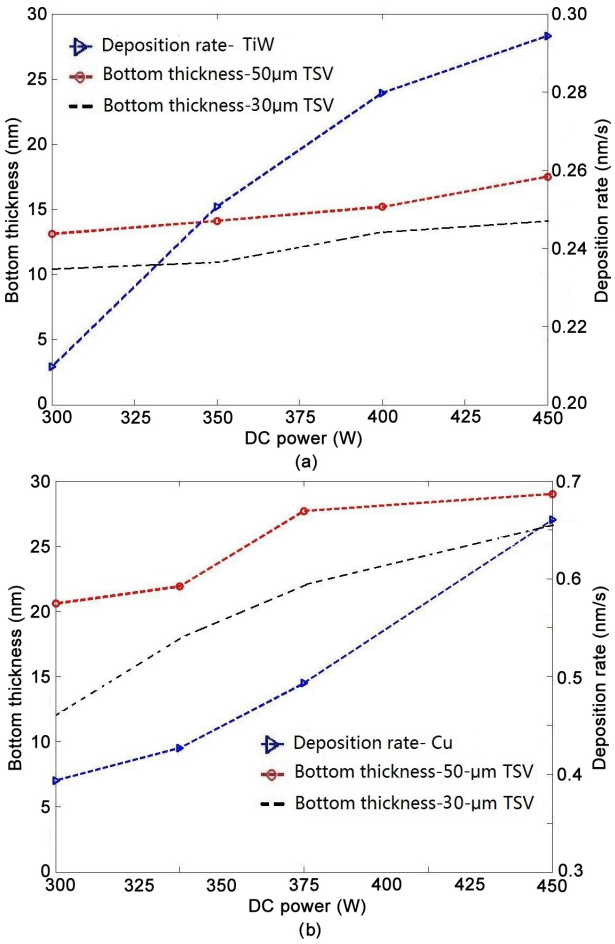

Fig. 11 Deposition rate and bottom thickness vs DC power: (a) TiW analysis; (b) Cu analysis.

into more ionized ions, the density of argon ions is higher, thus the deposition rate is improved. In addition, the large DC power between the target and wafer enhances the acceleration of argon ions and ion bombardment on metal targets. Therefore, 450 W is the optimized DC power both for TiW/Cu sputtering (500 W is the DC power limit for magnetron sputtering equipment).

4.5 Effect of substrate temperature on film coverage

To evaluate the effects of substrate temperature on film coverage performance, the substrate was heated to 300 ℃ before sputtering. Tables 2 and 3 present the detailed results with via diameters of 30 μm and 50 μm, respectively. By testing the 9 positions inside TSV with an aspect ratio of 3.6∶1, we see Cu thickness increases when the substrate temperature reaches 300 ℃. However, the effect of substrate temperature decreases when the aspect ratio rises to 5∶1.

Table 2 The thickness of Cu at different positions with via diameter of 30 μm at 20 °C and 300 °C. (nm)

Temperature	Position								
(°C)	1	2	3	4	5	6	7	8	9
20	673.1	434.9	206.9	61.2	29.5	6.0	5.1	12.0	11.7
300	682.0	450.1	222.7	74.3	33.1	7.0	8.1	14.4	13.1

Table 3 The thickness of Cu at different positions with via diameter of 50 μm at 20 °C and 300 °C. (nm)

Temperature	Position								
(°C)	1	2	3	4	5	6	7	8	9
20	655.7	463.8	227.3	87.5	32.2	23.5	33.0	19.0	21.6
300	708.1	519.1	333.8	103.5	49.5	30.2	29.0	32.1	35.0

As shown in Fig. 12, the Cu grain size of 348.7 nm achieved when substrate temperature is 300 ℃, is significantly bigger than that when the substrate is at room temperature. The main reasons are as follows. At a high temperature, the adatom diffusion on the substrate surface is enhanced, and the adatom desorption rate and nucleation rate all change exponentially, which controls the Cu grain size. From the laws of thermodynamics, the grain lives in a stable state when the grain diameter becomes bigger[18]. As the grain size increases, there is a significant decrease in the volume fraction of grain boundaries or interfaces, which can improve the electromigration resistance and continuity of the seed layer. Equation (2) demonstrates that film continuity improves with the increase of adatom sticking coefficient by heating the substrate during or after deposition[19].

As the surface coverage and structural details and the kinetic energy of the impinging particles are fixed, the sticking coefficient of TiW/Cu is determined by the substrate temperature. Therefore, the film sticking coefficient at 300 ℃ is much better than at the normal substrate temperature of 20 ℃. In addition, the surface diffusivity is also increased by increasing the temperature, which contributes to seed layer continuity.

In general, seed layer continuity is improved efficiently at high substrate temperatures. However, the effect is limited for high aspect ratio TSVs, e.g., AR = 5∶1.

4.6 TSV plating results with optimized parameters

In order to get a robust TSV interconnect during via filling, a comparison of seed layer thickness inside the via with optimized processing parameters is implemented systematically. As shown in Fig. 13, a sufficient seed layer can be achieved inside the via

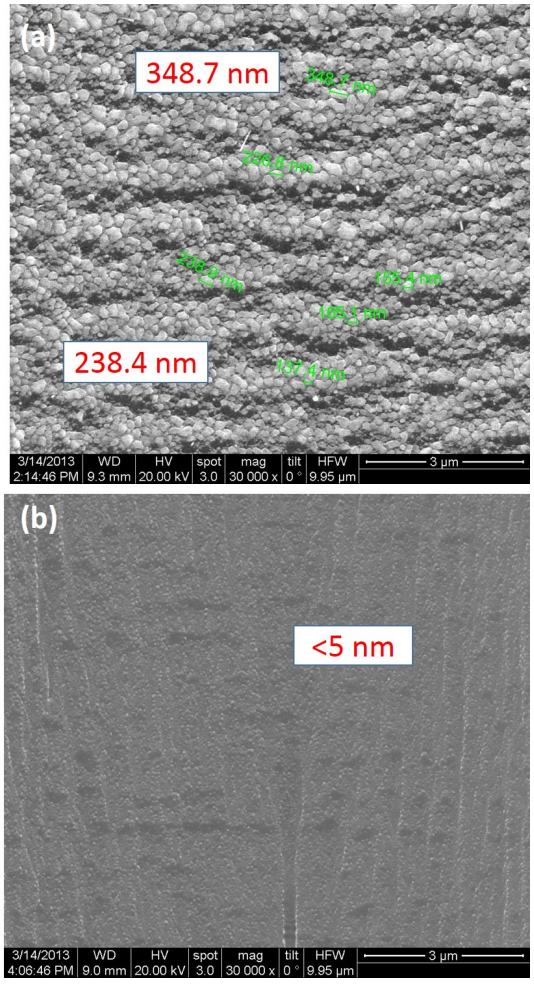

Fig. 12 Morphological surface of Cu films at different substrate temperatures by SEM: (a) 20 ℃; (b) 300 ℃.

by increasing deposition time. However, the thickness of Cu at the bottom of the via is not as improved as other factors. This is because the Cu particles do not have enough kinetic energy to reach the bottom of the via solely by increasing the deposition time. As shown in Fig. 13, DC power has advantages over the other three sputter factors, which could increase particle energy and drive higher deposition rates. Clearly, the Cu particles can easily reach the corner of the via bottom by gaining much more kinetic energy. As for the Ar pressure, appropriate pressure can improve film layer uniformity, while improper Ar pressure will reduce the continuity. Specifically, the suitable Ar pressure for TiW deposition is 8 mTorr and 5 mTorr for Cu deposition in this study. Temperature is a crucial factor for TiW/Cu deposition, so higher temperatures can improve the continuity of film layer inside the via. The discussion results are also suitable for TiW deposition.

Therefore, to improve the bottom thickness

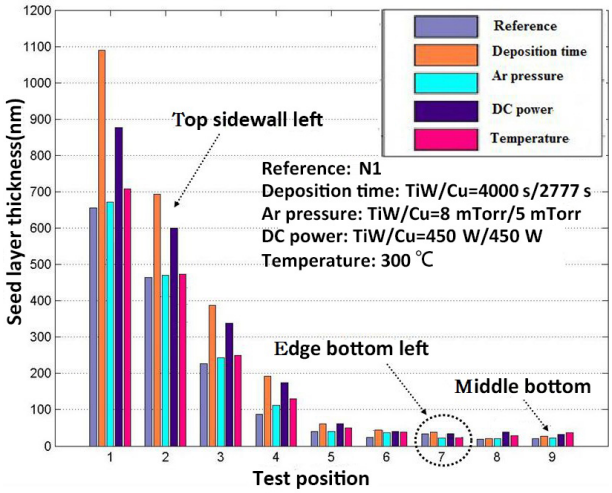

Fig. 13 Comparison of Cu thickness inside via with different parameters for 30-μm TSV (AR = 5∶1).

and continuity inside TSV, reasonable DC power is the primary factor for TiW/Cu magnetron sputtering, followed by Ar pressure and substrate temperature. Finally, the deposition time should be also considered in combination with cost. The following vias with a diameter of 30 μm will be discussed in detail. Sputter parameters are shown in Table 4.

With the optimized sputter parameters, robust TSV filling results with an aspect ratio of 5∶1 are illustrated in Fig. 14. Four positions inside the filled via are magnified to evaluate the TiW coverage. Results indicate that the optimized parameters are effective for filling TSVs with an aspect ratio of 5∶1.

5 Conclusions

In this work, systematic experiments were conducted to evaluate the effects of process parameters (deposition time, Ar pressure, DC power, and substrate temperature) on thin film coverage through conventional PVD sputtering. Among the four sputter factors, DC power is the most effective for improving TiW/Cu film coverage and deposition rate. The recommended DC power is 450 W for TiW and 450 W for Cu. The optimal Ar pressure is 8 mTorr for TiW and 5 mTorr for Cu, while improper Ar pressure can reduce

Table 4 The sputter parameters for 30-μm TSV.

Configuration	DT/s	AP/mTorr	P/W	t/℃
Baseline	2000/1666	4/6	200/200	20
Optimized	2000/1666	8/5	450/450	150

Notes: DT, deposition time; P, DC power; AP, argon pressure; t, substrate temperature.

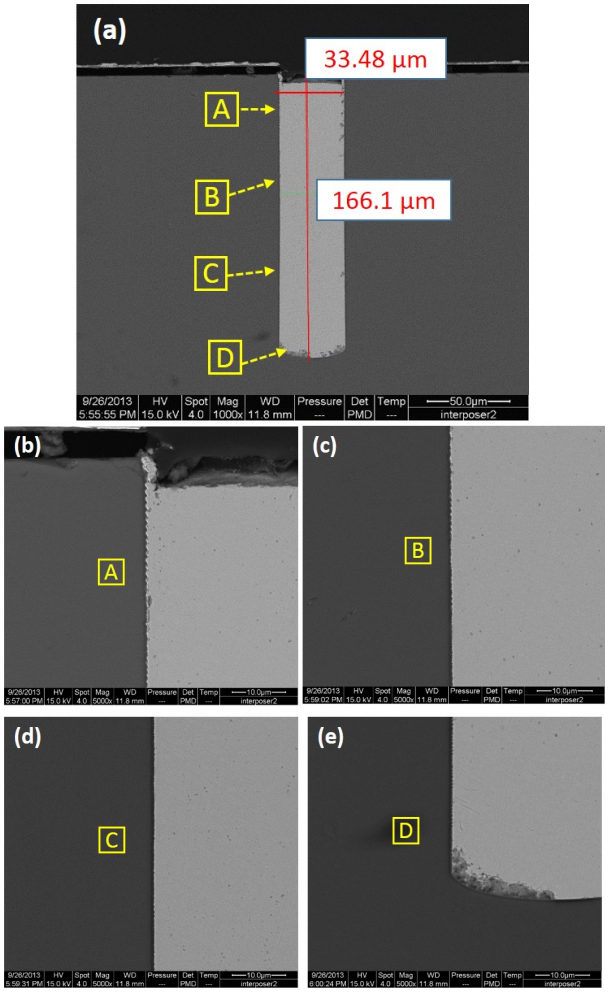

Fig. 14 TSV filling result with an aspect ratio of 5∶1: (a) Cross-section of TSV filling; (b) SEM image of top area A; (c) SEM image of middle area B; (d) SEM image of middle area C; (e) SEM image of bottom area D.

the effect. In addition, high substrate temperature can improve the continuity of film layers inside the via, especially for small aspect ratios. This is a good way to deposit thicker barrier/seed layers to achieve sufficient coverage inside a via for large diameter TSVs if cost and time consumption is not a big concern.

In conclusion, robust TSVs with an aspect ratio of 5∶1 are obtained with optimized magnetron sputter parameters. The influence of four parameters were analyzed and the conclusion could be used as a guideline to select appropriate parameter sets.

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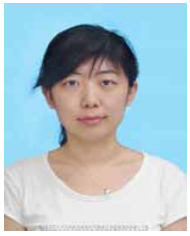
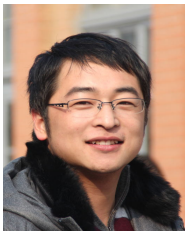
Tiwei Wei is currently a process and simulation engineer at Tsinghua Univerisity. He received his MS degree in optoelectronic engineering in 2012, from Chongqing University of Posts and Telecommunications, Chongqing, China. He studied as an exchange student in Institute of Microelectronics, Tsinghua University from November, 2011 to June, 2012. Since June, 2012, he joined Institute of Microelectronics, Tsinghua University as an engineer. His research focuses on 3-D integration technologies such as through-silicon-via, through-glass-via, and reliability of 3-D integration. He received "Outstanding Paper Award" as the first author in 13th International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP2012).

Jian Cai is currently an associate professor at Tsinghua University. He received his BEng degree in materials science and engineering, PhD degree in metallic materials and heat treatment, in 1993 and 1998, respectively, from Tsinghua University, Beijing, China. His main research interests include advanced packaging and system integration, focusing on system-in-package design and realization, through-silicon-via for packaging applications, etc.

Qian Wang is currently an associate professor at Tsinghua University. He received his PhD degree in 2000 from Tsinghua University, China. He was a postdoctoral fellow at RCAST (Research Center for Advanced Science & Technology), the University of Tokyo and NIMS (National Institute for Materials Science) in Japan from 2000 to 2003. His research focuses on advanced packaging technologies such as SiP, MEMS packaging and WLP, packaging reliability, and failure analysis.



Yang Hu is currently an engineer at Tsinghua University. She received her MS degree in materials science in 2006 from University of Science and Technology Beijing, Beijing, China. Her main research interest focuses on 3-D integration technology.



Lu Wang is now a master candidate in microelectronic engineering at Tsinghua University. He graduated from North China Electric Power University in 2011 with a BEng degree. He now focuses his research topics on TaN atomic layer depositon and its application in through silicon via and copper electroplating.

Ziyu Liu is currently a PhD candidate in microelectronic engineering at Tsinghua University. She received her BEng degree from Jilin University in 2010. Her main research interests include through silicon via, bumping technology, and Cu bonding interconnection.

Zijian Wu is currently a PhD candidate at Tsinghua University. He received his BEng degree in materials science and engineering in 2012 from Tsinghua University, Beijing, China. His main research interests include MEMS packaging and 3-D integration technology.