Low-Cost Energy-Efficient On-Chip Hotspot Targeted Microjet Cooling for High-Power Electronics

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***Abstract*— This article presents the design, fabrication, experimental characterization, and modeling analysis of the chip-level hotspot targeted liquid impingement jet cooling for high-power electronics. The hotspot targeted jet impingement cooling concept is successfully demonstrated with a chip-level jet impingement cooler with a 1-mm nozzle pitch and 300-μm nozzle diameter fabricated using high-resolution stereolithography (additive manufacturing). The computational fluid dynamics (CFD) modeling and experimental analysis show that the improved hotspot targeted cooler design with fully open outlets can reduce the on-chip temperature difference by 70% compared with the full array cooler at the same pumping power of 0.03 W. The local heat transfer coefficient can achieve 15 × 10^4 W/m^2 K with a local flow rate per nozzle of 40 mL/min, requiring a pump power of 0.6 W. The benchmarking study proves that the hotspot targeted cooling is much more energy-efficient than uniform array cooling, with lower temperature difference and lower pump power.**

***Index Terms*— Computational fluid dynamics (CFD), energy-efficient, hotspot, targeted cooling, temperature uniformity.**

I. Introduction

THERMAL management is becoming a primary design concern for high-power devices with the continuous scaling of the transistor size and increasing power density [1]. The localized heat flux can achieve values above 1 kW/cm^2 for submillimeter areas. These concentrated high heat flux values can cause localized hotspots (HSs) with very high peak temperature [2], which can adversely impact the device performance and reliability [3], [4]. In works of literature, many cooling solutions are investigated to minimize the maximum chip temperature [5], such as liquid cooling-based microchannel [6] and microjet heatsinks [7], which can be further enhanced by increasing the contact area with fin arrays [8] or porous media [9]. In addition, some compact two-phase cooling systems, such as micro heat pipes [10], are studied. However, these uniform cooling solutions for the complete chip surface or base plate area can result in excessive cooling in order to keep the maximum junction temperature below the specified maximum value in concentrated heat flux cases. Therefore, more energy-efficient cooling techniques should be developed by providing the targeted cooling on the local hotspots directly.

In the literature, several approaches have been proposed to eliminate the hotspots with high heat fluxes. To dissipate the high concentrated heat flux on the hotspots, diamond [11] or graphene [12] heat spreaders are applied to enhance the effective heat spreading capability. However, the cooling capacity is limited for high-power devices. Embedded thermoelectric cooling (TEC) with small size, high reliability, and low noise has great potential to provide reliable and localized cooling at hotspots [13] as they can be integrated into the heat spreader [14] or lid [15], embedded in the 2.5-D/3-D stacked chip package [16], [17], or placed directly on the backside of the device [18]. Droplet-based cooling of electronic hotspots without external pumps has been demonstrated with the control of electrostatically actuated droplets, referred to as digital microfluidics using planar [19] or vertical integration [20], [21] schemes. However, the drawback of the TEC cooling and droplet cooling is the overall low cooling efficiency, the high energy consumption [14], and the complex integration in the chip package.

In addition, liquid-based cooling solutions have been investigated to deal with the hotspots, including manifold microchannel (MMC) heat sinks with embedded microchannels [22]. The hotspot targeted cooling is achieved by optimizing the microchannel array; fine channels are designed over the hotspot locations, whereas coarse channels are present at the locations with lower background power dissipation, used as flow throttling zones to regulate flow in the different regions. The optimized cooler of [22] can reduce the maximum chip temperature nonuniformity by 61% to 3.7 °C for an average steady-state heat flux of 150 W/cm^2 in core areas (hotspots) and 20 W/cm^2 over remaining chip area (background). Microchannel cooler designs can be further optimized by varying the fin length and fin pitch in the

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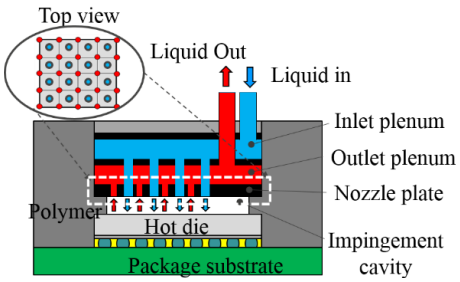

Fig. 1. Concept of bare die impingement jet cooling with uniform array cooling [27].

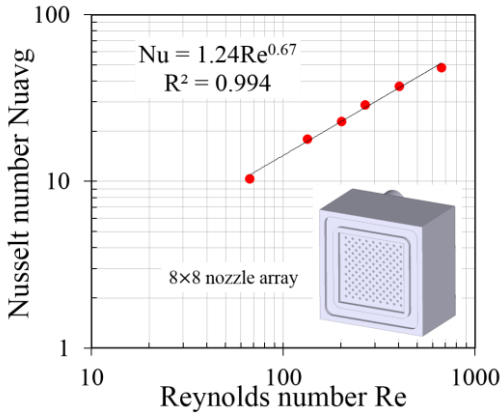

Fig. 2. Measurement results with uniform array cooling for 8 × 8 nozzle array cooler [30] under different local nozzle flow rates.

heat sink according to the local hotspot heat flux [23], [24]. The thermal performance of the microchannel coolers can be further improved by combining the microchannels with an impinging microjet array. This type of hybrid Si heat sink has been introduced as a package-level hotspot cooling solution [11], [25], for GaN-on-Si device in combination with a diamond heat spreader, achieving a high spatially average heat transfer coefficient of 18.9×10^4 W/m^2 K with a low pumping power of 0.17 W. However, these microchannel-based cooling technologies require expensive Si-based fabrication techniques, such as etching and lithography.

In this article, a low-cost energy-efficient hotspot targeted cooling solution with polymer-based impingement jet cooling is introduced. In Section II, the novel hotspot targeted cooling concept is introduced in detail and compared with the reference uniform array cooling. Furthermore, the thermal test vehicle and the dedicated experimental setup are discussed. In Section III, the hotspot targeted coolers are demonstrated and experimentally characterized as a proof of concept, benchmarking the improved performance with respect to the reference cooler. Next, in Section IV, full cooler level computational fluid dynamics (CFD) models are introduced for the detailed analysis of the flow and temperature distribution inside the cooler in order to investigate the internal thermal and flow behavior in detail. Next, the CFD modeling results are experimentally validated by thermal and hydraulic measurements. Finally, in Section V, the flow and heat transfer characteristics are analyzed based on the validated CFD models, and further improvements of the cooler geometry are discussed in order to increase the energy efficiency.

II. On-Chip Hotspot Targeted Cooling

A. Reference Cooler: Uniform Array Cooling

Bare die jet impingement cooling on the chip backside shown in Fig. 1 has lots of advantages over the mentioned cooling solutions in Section I. First, the direct cooling on the chip backside can achieve a very high cooling efficiency and lower thermal resistance by eliminating the thermal interface materials (TIMs). Second, the outlet flow within the cooling unit cell can be removed locally, resulting in a lower pressure drop [26] than microchannel cooling. Most importantly, microjet cooler with small form factor can be integrated within the chip or package level, which can increase the integration density of the system.

In our previous study, this concept has been demonstrated with the micromachining process [27], showing high cooling efficiency with a lower pressure drop and lower thermal resistance. The benchmarking study proves that multijet array cooling is more energy-efficient than other states of art liquid cooling solutions. It is also shown that the thermal conductivity of the cooler material has no big impact on the thermal performance of the impingement cooler, allowing to use a low-cost polymer-based cooler. The 3-D printing technology shows great advantages to fabricate low-cost polymer microjet coolers with complex internal 3-D geometries comparing with mechanical micromachining techniques [27]–[29]. With the high-resolution 3-D printing technology, microjet cooler with 8 × 8 nozzle array and 0.3-mm nozzle diameter was demonstrated [30]. In this session, the new measurement results under different flow rates are reported by using our 8 mm × 8 mm thermal test chip [29] with integrated heaters and temperature sensors. Fig. 2 shows the Nu–Re correlation for the 8 × 8 nozzle array cooling. It can be seen that Nu shows as a function of the Re with a power-law trend with an exponent of 0.67, which is listed as follows:

$$\mathrm{Nu} = 1.24 \cdot \mathrm{Re}^{0.67} \tag{1}$$

where Nu is based on the measured averaged chip temperature.

The hydraulic characteristics lengths of the dimensionless number Nu and Re are both based on the inlet nozzle diameter di.

With the Nu–Re correlation, the local heat transfer coefficient htc also shows as a function of the local flow rate per nozzle $\dot{V}$ with a power-law trend with an exponent of 0.67, where the local flow rate is calculated based on the total flow rate, which is listed as follows:

$$\dot{V} = \frac{\dot{V}_{\mathrm{tot}}}{N \times N} \tag{2}$$

where $\dot{V}_{\mathrm{tot}}$ is the total flow rate for the cooler, and $\dot{V}$ is the local flow rate per nozzle. Also, $N \times N$ is the inlet nozzle array. The parameter N is a fixed number equal to 8 throughout the analysis since the uniform nozzle array design is an 8 × 8 nozzle array in the considered case. As shown in Fig. 2, the measured maximum heat transfer coefficient can

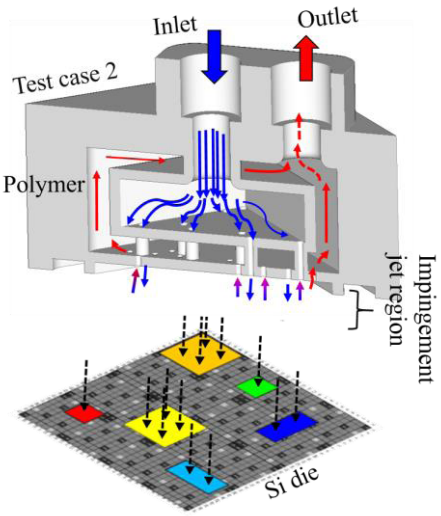

Fig. 3. Concept of hotspot targeted liquid impingement cooling.

be achieved as 7.39×10^4 W/m^2 K with a local flow rate per nozzle of 15.63 mL/min, resulting in a total flow rate of 1000 mL/min. The pressure drop measurement result for the full nozzle array cooling with an 8×8 nozzle array is listed in Fig. 10(b). However, the previous studies are focused on the uniform power dissipation with uniform nozzle array cooling. In Section II-B, a hotspot targeted cooling concept will be introduced for nonuniform power, which can be made even more energy-efficient.

B. Hotspot Targeted Cooling Concept

Additive manufacturing enables the customization of the cooler design to match the power dissipation pattern of the chip in order to increase cooling efficiency [28]. In the case of hotspot power dissipation patterns, the location of the impinging jet nozzles that eject the coolant onto the chip can be aligned to the location of the hotspots. The main idea of hotspot targeted cooling is to focus the cooling solution, at the location where it is needed. In the areas outside the hotspots, a lower nozzle density is designed to cover the area with lower heat flux values for the background power dissipation. In the extreme case where no background power is present, the nozzles outside the hotspot area can be omitted since no power generation is present. In this way, a higher local cooling flow rate will be provided to the chip locations with higher power densities, resulting in a selective cooling of the chip area, rather than a uniform cooling across the whole chip surface. Since the constriction of the coolant to these selected regions will result in higher heat transfer rates as well as higher required pressure drop values, a detailed experimental and numerical analysis is presented in Section III. The concept of the hotspot targeted liquid impingement jet cooling is schematically shown in Fig. 3 for the case with several hotspots and no background power.

C. Programmable Thermal Test Chip

In order to experimentally capture the local temperature profile of the hotspots with sufficient accuracy and to assess

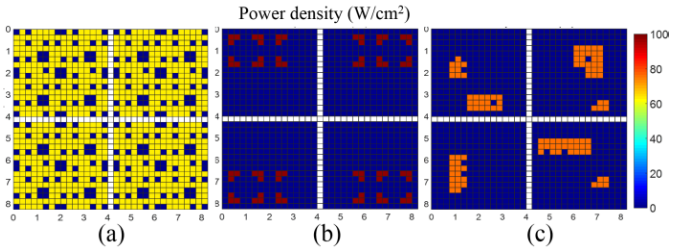

Fig. 4. Test cases for the hotspot cooling with different power density maps. (a) Reference case with the quasi-uniform heating pattern. (b) Test case 1 with the regular pattern. (c) Test case 2 with various hotspot sizes.

the effectiveness of the cooler, a high spatial resolution and programmable thermal test chip, referred to as Packaging Test Chip version Q (PTCQ) [29], is used. The chip with an area of 8×8 mm^2 contains a 32×32 array of 240×240 μm^2 square cells with additional peripheral circuits with I/O and control cells in the central cross of the chip. All the cells in the 32×32 arrays contain diodes as temperature sensors, fabricated by front-end-of-line (FEOL) semiconductor processing, allowing the measurement of the full-chip temperature cells also contain metal meanders fabricated in the back end of line (BEOL). These heater cells are individually ON/OFF controlled by local flip-flop transistors, allowing custom power dissipation patterns ranging from local hotspots to quasi-uniform power dissipation with 75% coverage of the thermal test chip, as shown in Fig. 4(a). The maximal power for a single heater cell is 47.6 mW at 1 V with the heater cell area of 240×240 μm^2, resulting in a maximal heat flux per cell about 82.6 or 100 W/cm^2 at 1.2 V. The temperature sensitivity is calibrated as ± 0.02 mV/°C for a current of 5 μA in the temperature range between 10 °C and 75 °C. For the assessment of the hotspot targeted cooling, two hotspot case studies have been defined based on the heat generation capabilities of the test chip as follows:

1) test case 1 with a regular hotspot pattern, mimicking the design of a multicore processor [see Fig. 4(b)];
2) test case 2 with various hotspot sizes, mimicking a power electronics die [see Fig. 4(c)].

For test case 1 with the regular hotspot pattern, there are 72 heater cells activated with a total heater area of 4.15 mm^2 for the 24 heat sources. For test case 2 with various hotspot sizes, the total number of the activated heater cells is 127, with a heater area of 7.32 mm^2. The power density scale for the three different power maps (for 1 V) is shown in Fig. 4. The power and power density are different for all three cases. The test chip is powered by applying a voltage and by choosing which heater cells are activated. In the experiments, a constant voltage of 1 V is applied at the package. The actual power in the heater cells (and the local voltage drop) depends on the series connection of parasitic resistance and heater resistance array, which acts as a voltage divider, and on the connections in the package substrate depending on the metal line connections between the heater cell and the contact pad. For the example of 1 V of applied voltage on the package, the actually measured power dissipation in the heater cells is given as follows.

1) *Hot Spot Test Case 1:* Total power is 4.1 W and power density is 98 W/cm^2.
2) *Hot Spot Test Case 2:* Total power is 5.5 W and power density is 75 W/cm^2.
3) *Uniform Reference Case:* Total power is 30 W and power density is 62.5 W/cm^2.

The power values/densities, in this article, are limited to a small value (<10 W), which is not correlated with the modern high-power CPUs/GPU in 100–200 W. However, the extracted thermal resistance or heat transfer coefficient can be scaled to high power value. Based on the power densities' value q, the temperature increase can be estimated by the equations $q = h * \Delta T$.

The steady-state chip temperature distribution can be extracted by measuring the voltage across the 32 × 32 array diode sensors. The measurement uncertainty for the sensor and heater voltages is 1 and 1.6 mV, respectively. The inlet temperature of the liquid (DI-water) is kept as 10 °C in the experiment by using a heat exchanger in the closed loop to make sure that the thermal test chip works in the safe temperature regime. However, having an inlet temperature below ambient may cause condensation issues for real electronic applications while also requiring a chiller. Therefore, the temperature results shown in this article are reported as temperature increase values with respect to the inlet temperature, which are also valid for ambient inlet temperature or higher inlet temperatures. The sensitivity of the diode temperature sensor is measured based on more than 500 diodes, showing 95% confidence level with ±1.5%. For the uncertainty analysis of the reported quantities, the uncertainty of all the measurement devices has been considered, and the theory of measurement error propagation has been used. The considered measurement uncertainties are as follows:

1) the measured chip power (±0.1%);
2) the average chip temperature measurement (±1.5%);
3) inlet temperature measurement (±1%);
4) the measured nozzle diameter (±3.5%);

Therefore, the propagated measurement uncertainty results in a value of ±3.94% for the reported heat transfer coefficient. The pressure measurement uncertainties are based on the accuracy of the pressure transducer. The flow rate measurement errors are based on the accuracy of the flowmeter.

III. Proof of Concept: Hotspot Targeted Cooler

A. Demonstration of 3-D Printed Cooler

The hotspot targeted cooler demonstrator is fabricated using additive manufacturing. Polymer-based high-resolution stereolithography (SLA) with the specified fabrication tolerances of 0.05 mm in the x/y-directions and ±0.13 mm in the z-direction has been used. This results in the successful fabrication of the cooler with the nozzles' diameter of 300 μm and a pitch of 1 mm using the water-resistant Somos WaterShed XC material [31], which shows acrylonitrile butadiene styrene (ABS)-like properties. The heat deflection temperature (HDT) of the printed material is around 60 °C [31]. Therefore, the temperature of the coolant should be below 60 °C to remain in the safe temperature range for the cooler material. Moreover, the SLA-based 3-D printer Formlabs Form 2 is used for the printing of the coolers. For a cooler size of 14 mm × 14 mm × 8 mm, the total time required to produce the part is about 8 h. Schematics of the designed hotspot targeted cooler versions for the two test cases are shown in Fig. 5, revealing the internal cooler geometry. The cavity height is designed as 0.6 mm. The number of the inlet nozzles for test case 1 is 24, while it is only 15 for test case 2 compared with 64 for the full array cooler. The location of the nozzles has been aligned to the location of the hotspots of Fig. 4(b) and (c). The top row of Fig. 6 shows a bottom view of the designs of the nozzle plate, while the bottom row shows a comparison with the photographs of the actually fabricated demonstrators. The uniformity of the printed nozzle diameter can be measured from the bottom view of the cooler, showing only a 5% difference. The nozzle diameters show a variation between 541 and 607 μm, where 570 μm is the average of the measured diameter values and the standard variation is 13 μm. The demonstrators are first optically evaluated with a microscope. The nozzle shapes exhibit a nice circular profile. The measurement of the fabricated nozzle diameters shows a deviation of only 5% compared to the nominal design value (570 versus 600 μm). Moreover, the internal structure of the cooler can be evaluated by scanning acoustic microscopy (SAM) [28], in order to reveal residual uncured resin or blocked nozzles.

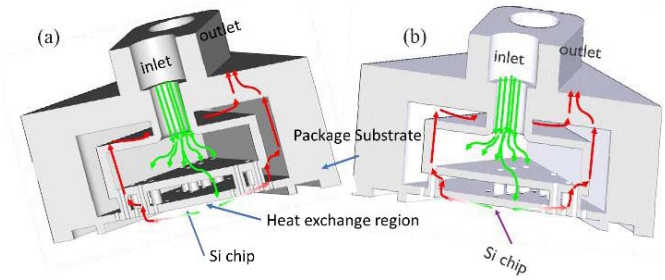

Fig. 5. Cross section of the computer-aided design (CAD) designs of the two test cases. (a) Test case 1. (b) Test case 2.

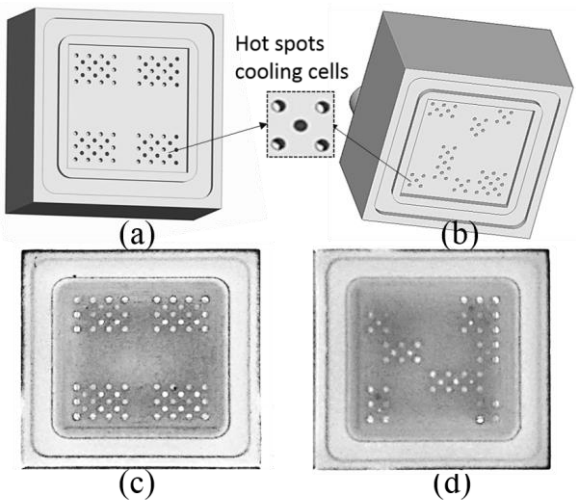

Fig. 6. Bottom view of the hotspot targeted coolers revealing the nozzle array for (a) test case 1 and (b) test case 2. Photographs of the nozzle plate of the fabricated coolers for (c) test case 1 and (d) test case 2.

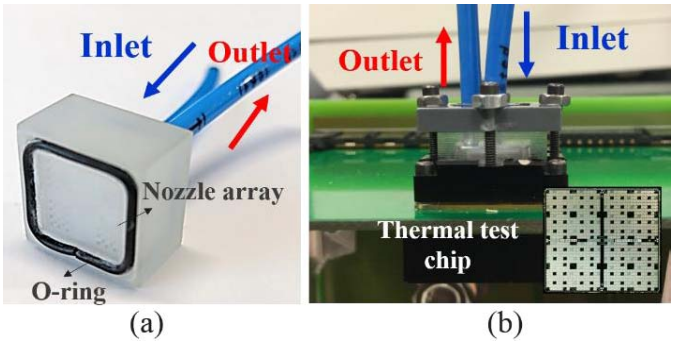

Fig. 7. Cooler assembly. (a) Hotspot cooler for regular pattern with O-ring placement. (b) Assembly of the cooler on the thermal test chip and PCB test board.

B. Thermal Characterization

For the assembly of the cooler, an O-ring, placed inside a groove on the cooler's surface as shown in Fig. 7(a), is used to seal the connection between the cooler and the package substrate in order to prevent leakage of the liquid coolant. In the assembly, the microbump array between the die and the package has been underfilled. This underfill material protects the microbumps from the liquid coolant. The thickness of the O-ring is 1 mm, while the groove depth is 0.6 mm. After the placement of the sealing ring, the dedicated hotspot cooler demonstrator is mechanically assembled on the package substrate with the advanced thermal test chip by using a plastic socket, as shown in Fig. 7(b). The assembled cooler is finally connected into the closed-loop test setup enabled with accurate flow rate and pressure drop measurement systems.

In the first set of experiments, the heat dissipation patterns on the chip, shown in Fig. 5(b) or (c), are activated, while the full-chip temperature map is measured for a certain flow rate once the steady-state condition has been reached. The chip temperature is extracted at the chip FEOL, which is the same location as where the diodes are, and the junction in the application.

The measured total chip power for test case 1 with a regular hotspot pattern is 4.1 W. For test case 2 with various sizes of hotspot, the measured total chip power is 5.5 W. The power for the reference case with uniform heating is set as 30 W. For both test cases, the chip temperature profile is compared between the reference full array cooler (see Section II) and the respective hotspot targeted cooler (see Section III) for the same coolant flow rate.

For the coolant heat removal percentages, we performed the thermal measurements of the packages without cooling applied. In the experiments, the results show that the percentage of heat loss through the package is limited to only 2%–5% and the majority of the heat is removed through the top side of the chip, and since the power values for test cases 1 and 2 are only 4.1 and 5.5 W, respectively, the heat loss through the package and convection can be considered very similar. At these temperature values (15 °C average chip temperature), radiation can be neglected.

In Fig. 8, the measured temperature maps are compared for a total flow rate of 600 mL/min. For a more detailed

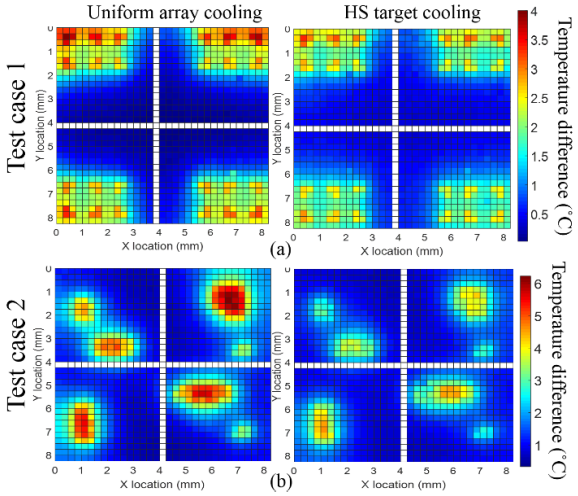

Fig. 8. Measured temperature distribution for uniform array cooling and HS cooling with (a) test case 1 regular hotspot pattern and (b) test case 2 with various hotspot sizes at a flow rate of 600 mL/min.

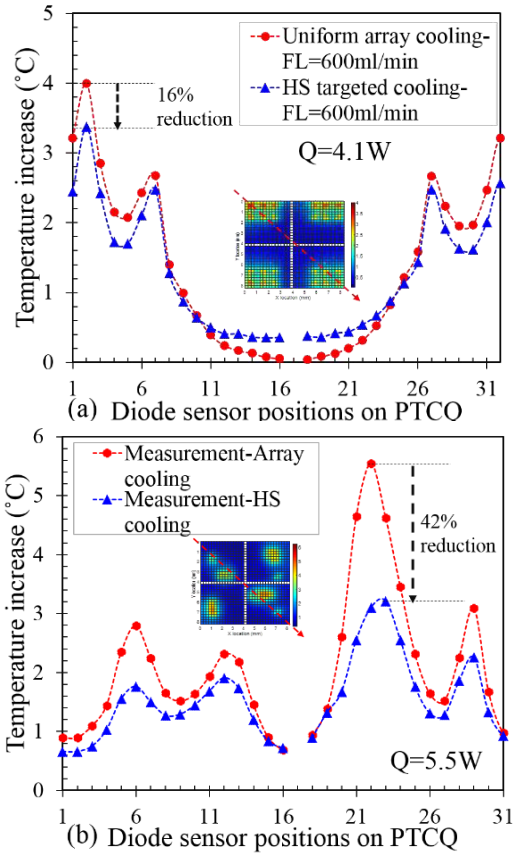

Fig. 9. Temperature profile comparison for (a) test case 1 regular hotspot pattern and (b) test case 2 with various hotspot sizes with the reference cooler. Note: Temperature increase is with regard to the inlet fluid.

comparison, the temperature profile is plotted across the test chip diagonal, as shown in Fig. 9. The temperature measurements show a peak temperature reduction of 16% and 42% at a flow rate of 600 mL/min compared to the full array cooler for the targeted hotspot coolers of test cases 1 and 2, respectively, indicating that concentrating the liquid coolant on the locations where it is needed can result in a significant

reduction of the chip peak temperature due to the locally increased coolant flow rate. This is, however, achieved at the cost of an increase in required pressure drop. The pressure drop will be characterized experimentally in Section III-C, while the flow distribution impact will be discussed in Section V-A.

C. Pressure Drop Measurements

For the hydraulic characterization of the hotspot targeted cooler, a mini Cori-FLOW mass flowmeter with model number M15-RGD-22-0-S and a differential pressure gauge (EL-PRESS) with model number P506C-21KR-RGD-22-V are used in a closed-loop setup to control or measure the flow rate and pressure drop. Mass flow can be measured in the range of 378–11 000 mL/min and with an accuracy of ±0.2%, while the pressure drop across the cooler can be measured with an accuracy of ±0.5% FS in the range between 0.2 and 5 bar. The coolant in the flow loop is pumped by a magnetically coupled gear pump with a maximum flow rate of 11 000 mL/min and a maximum pressure of 11.5 bar.

As shown in Fig. 10(a), the inlet and outlet of the cooler are connected with small tubes for the whole flow loop connection. Therefore, the pressure drop of the inlet/outlet tube and connection is included in the measured pressure drop. The modeling results show that the pressure drop of the cooler is smaller than the tube connection part; therefore, a deembedding technique can be used to measure the pressure of the cooler only, without the tube connection. Since the pressure drop over the tube is linearly proportional to the tube length, the pressure drop between the inlet and the outlet connection of the cooler can be estimated by measuring the pressure drop for the different tube lengths and extrapolating to zero tube length. The pressure drop over the three coolers has been measured for controlled flow rate values in the range between 50 and 1000 mL/min. As shown in Fig. 10, the measured pressure drop for the uniform 8 × 8 array cooler is lower than for the other cooler under the same flow. The pressure drop of hotspot targeted cooler for test case 1 is 3.2 times higher than the uniform array cooling, while the pressure drop for test case 2 is 5.9 times larger under the flow rate of 1000 mL/min. The increase in the pressure drop is due to the reduction of the number of nozzles and the additional hydraulic constriction resistance in the inlet plenum.

In summary, the thermal and hydraulic measurements show that the hotspot targeted cooler can improve the cooling efficiency toward the hotspots, however, at the expense of an increase in pressure drop. In Section IV, the hydraulic behavior will be investigated in more detail using validated CFD models.

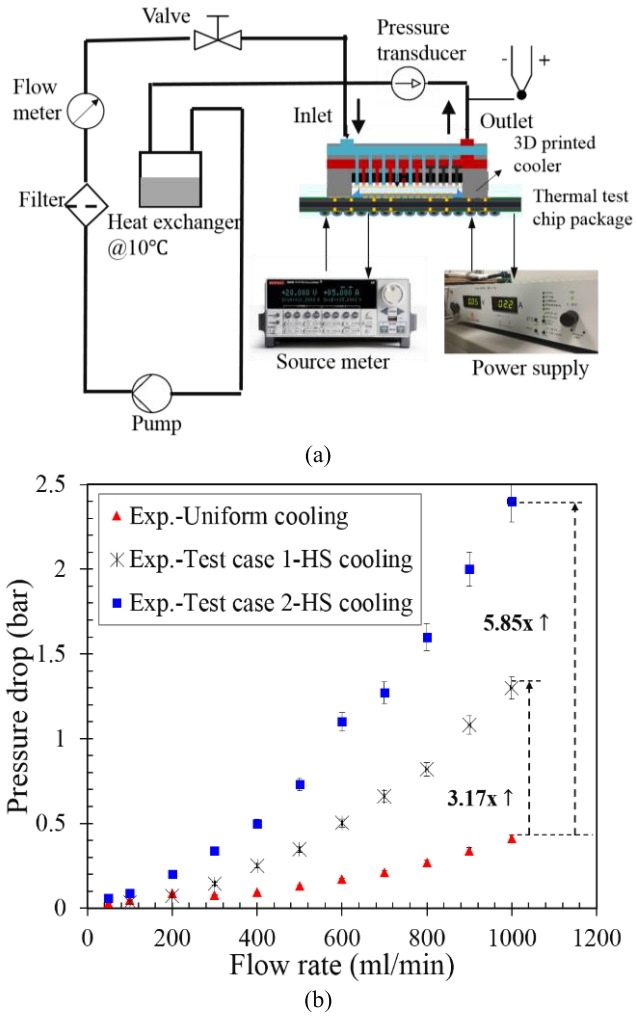

Fig. 10. (a) Schematic of the thermal/flow loop measurement system and (b) the pressure drop measurements for the reference cooler and the two versions of the hotspot target cooler.

IV. Modeling Methodology and Validation

A. Full Cooler Level CFD Model

System-level pumping power is an important factor for the design of the liquid cooler from an energy consumption point of view. Unit cell-level models on the level of an individual jet nozzle provide an interesting insight in the thermal and hydraulic behavior of the multijet cooler [27]; however, they can only predict the pressure drop between the local level inlet and outlet nozzles on the nozzle plate. In order to assess the cooler hydraulic behavior and to extract the pressure drop between the inlet and the outlet, full cooler level CFD models are required. Furthermore, these full cooler level CFD models can be used to optimize the geometry of the inlet plenum and outlet plenum in order to reduce the pressure drop in the cooler.

Fig. 11 shows the full cooler model geometry, extracted from the CAD design file. The model is based on a steady-state conjugate heat transfer CFD model using ANSYS software, which considers the heat conduction in the solid structures and heat conduction and convection in the liquid domain in the system. Actually, the solid domain in the CFD model is the silicon die part and not the solid part of the plastic manifold. Our previous study [27]–[29] showed that the thermal conductivity of the cooler material has no impact on the modeling results for temperature distribution in the Si chip, and no difference was found using a thermal insulation boundary condition on the surface of the fluid domain inside

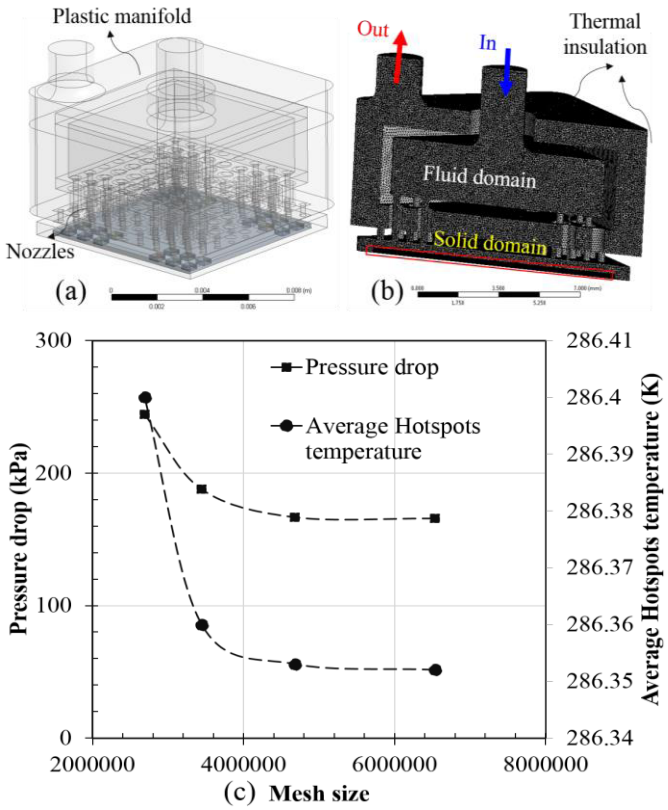

Fig. 11. Full cooler level CFD model. (a) Transparent view of the cooler. (b) Cross section of the meshing with test case 1. (c) Mesh sensitivity analysis with CFD model of test case 1.

the cooler geometry. Therefore, the presented CFD model does not include the plastic part of the cooler. In addition, for the interface between the fluid domain and the solid domain (silicon die), there is a boundary layer mesh between the solid part and the fluid part. For the boundary layer mesh, the first layer thickness and grow ratio are all set in order to make sure the mesh transition as smooth as possible. The studied cooler flow rate ranges from 100 to 1000 mL/min, which corresponds to a Reynolds number of 100–2000, based on the inlet nozzle diameter. The typical range for the Re number for the transition from laminar to turbulent flow is 1000–3000 [26]. Therefore, the transition shear stress transport (SST) model is chosen as the turbulent model in the CFD simulations, which can cover the laminar and transition flow regimes with good accuracy for jet impingement flows [26]. The "SIMPLE" algorithm is used as the solution method. For the numerical scheme, the QUICK scheme is chosen for the discretization. In order to capture the temperature distribution map with the hotspots, a sufficiently detailed mesh of the heaters is required in the model [29]. In Fig. 11, the full-level CFD model of hotspot targeted cooler is shown and the mesh details are shown in a cross section of the modeled geometry. The results of the mesh independent analysis for the full cooler CFD model are shown in Fig. 11(c), performed for the regular hotspots cooler of case 1, at a fixed flow rate of 1000 mL/min. It is observed that the mesh for a number of elements between 4.5 and 5M is mesh-independent. Also, the truncation error estimation from the Richardson extrapolation [32] is around 0.28% and can be used for the modeling study. Since the critical region with the nozzle diameter is the same, therefore, the meshing sensitivity is also applicable for other cases. Based on the meshing sensitivity analysis, the meshing size of the fluid domain is set as 0.12 mm, while the meshing size is 0.04 mm for the solid domain. The first layer thickness of the boundary layer is set as 1e−3 mm in Z with ten layers above the fluid/solid interface, and the layer growth rate is set as 1.2. The total element number is 4.5–5M.

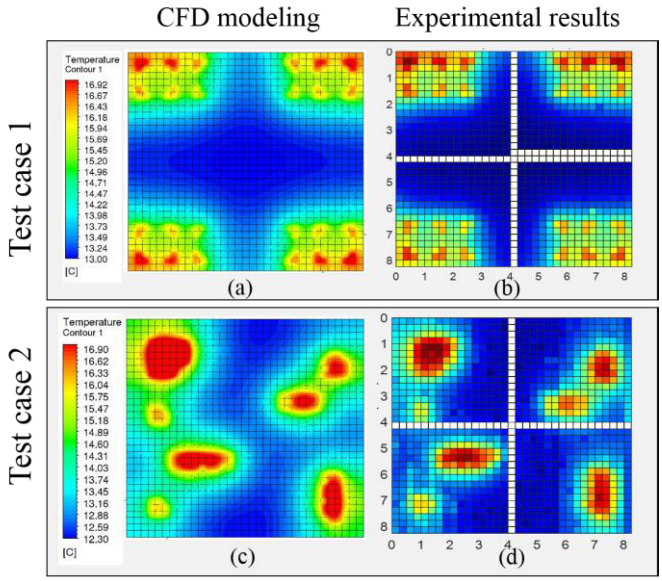

Fig. 12. Temperature map distribution comparison of test case 1 with chip power of $Q = 4.1$ W. (a) CFD modeling and (b) experimental results; test case 2 with the chip power of 5.5 W. (c) CFD modeling and (d) experimental results (flow rate = 600 mL/min).

For the boundary conditions of the model, the inlet temperature is set at 10 °C. A constant heat flux of 98 W/cm^2 is applied to the hotspot areas for test case 1, while the applied heat flux for test case 2 is 75 W/cm^2. To match the measurement conditions, a constant velocity is applied on the inlet boundary, while the boundary condition for the outlet pressure is set to $P_{\text{out}} = 0$ Pa. The fluid and solid interface is set as a coupled boundary condition. Since the cooler material is plastic with low thermal conductivity, the boundary walls of the internal cooler channels are assumed to adiabatic walls. This assumption has been validated by full cooler level simulations with different materials, showing no significant impact of the cooler material conductivity or the adiabatic boundary condition. The fluid properties and silicon die properties are not temperature-dependent.

B. Thermal and Hydraulic Model Validation

The temperature distribution map comparisons between the full cooler level CFD modeling and the experimental results for test cases 1 and are shown in Fig. 12 with a total power dissipation of 4.1 and 5.5 W for a flow rate of 600 mL/min. In general, the comparisons for the temperature map show good qualitative agreement between the measurement and simulation results. For the detailed comparison of test case 1,

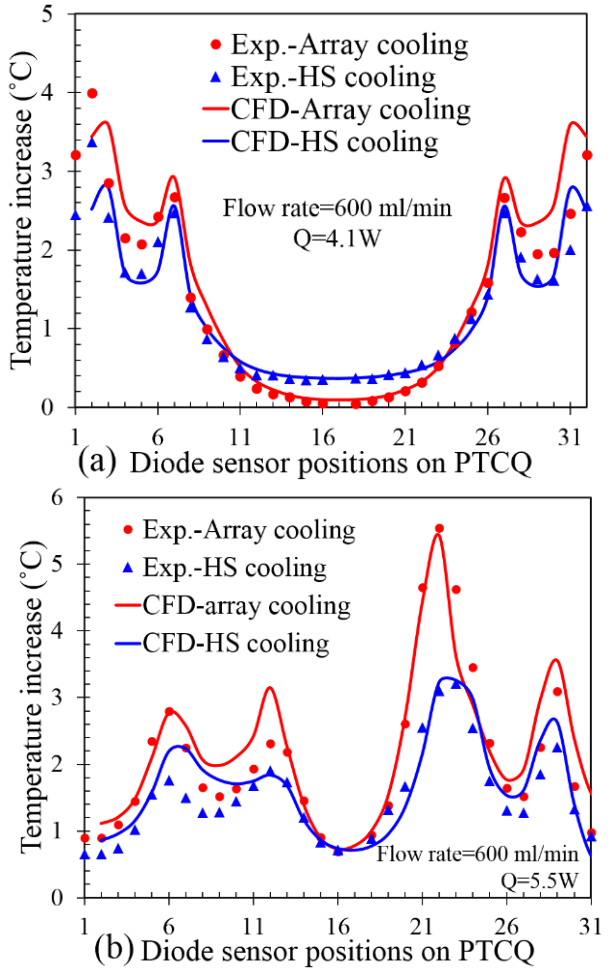

Fig. 13. Temperature measurement results and full cooler CFD model comparison for (a) test case 1 and (b) test case 2.

the temperature profile is plotted across the chip diagonal in Fig. 13(a). It can be seen that the model captures the temperature peaks and the area without power very well and also shows good agreement for the temperature profile. Moreover, the average difference between the simulated average chip temperature and the averaged chip temperature based on all 1024 temperature sensors is less than 3% for the uniform nozzle array cooler, while the average difference is 7% for the targeted hotspot cooler. The asymmetrical temperature measurement map shown in Fig. 13(a) is due to the asymmetrical placement of the outlet tube connector.

For the temperature profile of test case 2, shown in Fig. 13(b), the comparison also shows good agreement with the measurements and simulation results. For the averaged chip temperature in test case 2 calculated from Fig. 12(b), the comparison between simulation and measurement of the average chip temperature shows 6% and 9% average difference for the uniform array cooler and the targeted hot spot cooler, respectively.

As shown in Fig. 13, the hotspot cooler simulations have much higher deviation compared with the uniform case. This is because the CFD model is a simplified model where the bottom substrate and solder connections are presented as a boundary condition with an equivalent heat transfer coefficient.

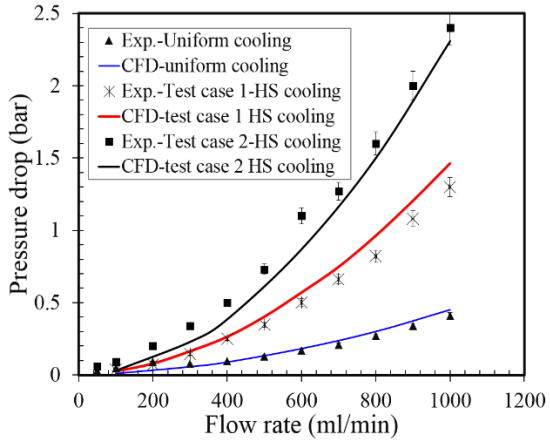

Fig. 14. Experimental and CFD modeling comparison for the pressure drop under different flow rates.

In case of the uniform heating and cooling, the heat transfer in the silicon die is primarily 1-D vertical, which is accurately captured by the simplified model. In the case of the hotspots, there is also a significant lateral spreading in the silicon. It could be possible that this lateral spreading is not completely captured.

Fig. 14 shows the comparison of the simulated pressure drop between the inlet and outlet connector and the experimental measurements for the three considered cooler designs. The simulated pressure drop shows a 12.3% average difference from the measured pressure drop at the flow rate of 1000 mL/min for test case 1. In general, the modeling results for uniform array and HS targeted cooling show good agreement with the experimental results, showing an average difference smaller than 13%.

Based on the acceptable errors of the full CFD cooler model compared with the experimental data, the CFD models with different cooler configurations are successfully validated. The validated CFD models are applied in Section V to assess the thermal performance gains for design improvements and for the tradeoff between the thermal performance improvement and the pressure drop penalty in the hotspot targeted cooler.

V. Thermal/Hydraulic Modeling Analysis

A. Local Flow Rate Analysis

For the local flow rate analysis, a unit cell approach is used as a first estimation to assess the improvement in cooling at the targeted chip areas. Based on the measurement data with 1×1 mm^2 cooling unit cells shown in Fig. 2, the relation between the local heat transfer rate htc and the local inlet nozzle flow rate $\dot{V}$ is shown with a power-law trend with an exponent of 0.67, derived from (1). Therefore, the expected heat transfer coefficient htc* for the hotspot cooler can be extracted as follows:

$$\text{htc}^* = m^{0.67} * \text{htc} \tag{3}$$

$$\dot{V}^* = m \cdot \dot{V} \tag{4}$$

$$m = \frac{N^2}{M}. \tag{5}$$

TABLE I
SIMPLIFIED THERMAL ANALYSIS USING UNIT CELL APPROACH

Case item	No.	Ratio m	$\dot{V}^*$ (ml/min)	htc^* (W/m^2 K)
Reference case	64	1	9.4	5.7×10^4
Test case 1	24	2.7	25	11.1×10^4
Test case 2	15	4.3	40	15.1×10^4

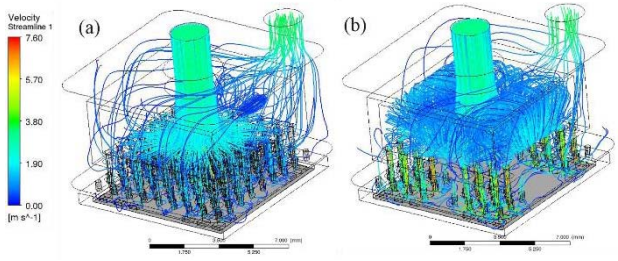

Fig. 15. Flow streamline distribution of hotspots targeted cooler with test case 1. (a) Uniform array cooling. (b) Hotspots targeted cooling (flow rate = 600 mL/min).

The hotspot area is used for the estimation of the local heat transfer coefficient that is mainly used as a relative comparison with the global heat transfer coefficient.

Similarly, the expected pressure drop for the targeted cooler is shown as follows:

$$\Delta p \sim m^2 * \dot{V}^2 \tag{6}$$

where $\dot{V}$ is the averaged local flow rate per nozzle and $\dot{V}^*$ is the averaged local flow rate for the hotspot targeted cooler. N^2 is the total inlet nozzle number with the array cooler. M is the total inlet nozzle number for the hotspot targeted cooler, and m is defined as the ratio between N^2 and M.

Table I shows the simplified thermal analysis results for the three test cases. Based on the heat transfer coefficient relation in (3), the inlet velocity per nozzle is 9.4, 25, and 40 mL/min for the reference uniform array cooler, test case 1, and test case 2 under a total flow rate of 600 mL/min. The achieved heat transfer coefficient for uniform array cooler is measured at 5.7×10^4 W/m^2 K with the local flow rate per nozzle of 9.4 mL/min. Therefore, for the same measured total flow rate, the achieved heat transfer coefficient for test case 2 is expected to be 15.1×10^4 W/m^2 K with the local flow rate per nozzle of 40 mL/min, at a pressure drop of 1.1 bar.

Using the full CFD model, the detailed temperature, velocity, and pressure drop information inside the dedicated cooler can be extracted. As for the simulation results of the hotspot targeted cooling, the flow streamlines inside the cooler are shown in Fig. 15. More flow recirculation is observed inside the hotspot targeted cooler since the flow is concentrated into the reduced number of inlet nozzles. It is also observed that the velocity in the nonheating area is lower since the outlet flow is removed locally through the cooling unit cells near the hotspot areas.

It is expected that the higher local heat transfer coefficient compared to the uniform array cooling case is due to the higher local flow rate with a smaller number of targeted inlet nozzles.

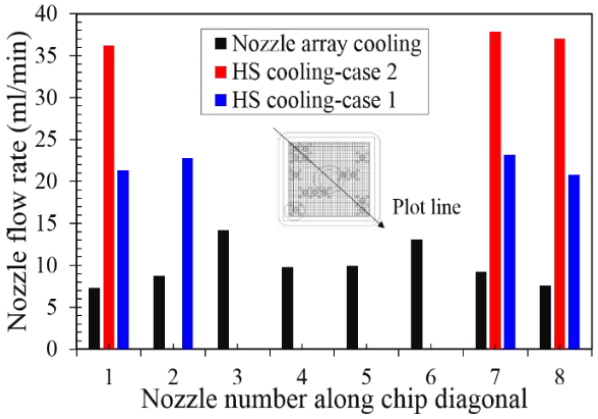

Fig. 16. Nozzle flow rate per nozzle along with the chip diagonal for the three test cases (flow rate = 600 mL/min).

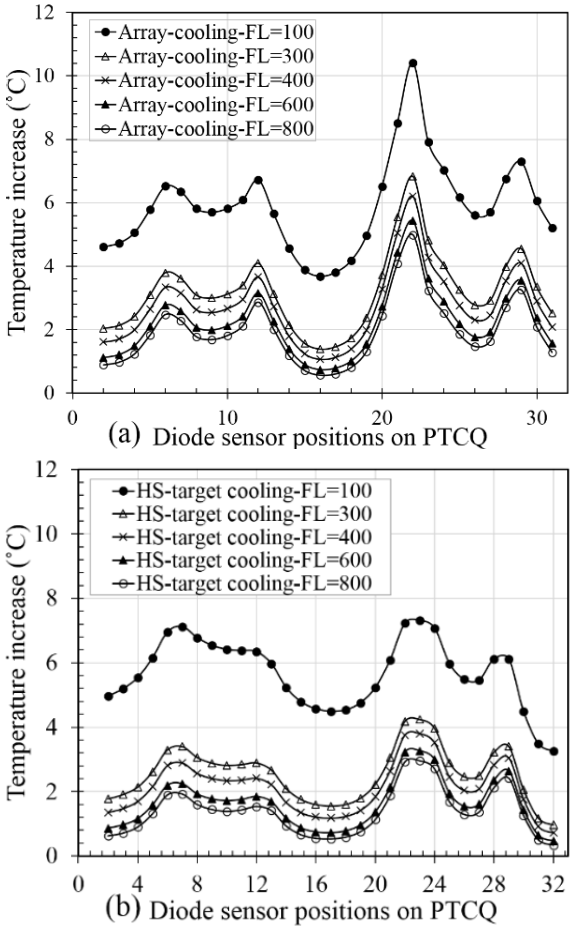

Fig. 17. Temperature profile comparison under different flow rates for test case 2 with (a) CFD modeling results of uniform array cooling and (b) CFD modeling results of hotspots target cooling ($Q = 5.5$ W).

Therefore, the local flow rate for the individual inlet nozzles along the chip diagonal is plotted in Fig. 16.

B. Temperature Uniformity Analysis

Given the good agreement between CFD and measurement results, the CFD models are used to assess temperature uniformity for different flow rates. The simulated temperature profiles of the uniform array cooling and hotspot target cooling

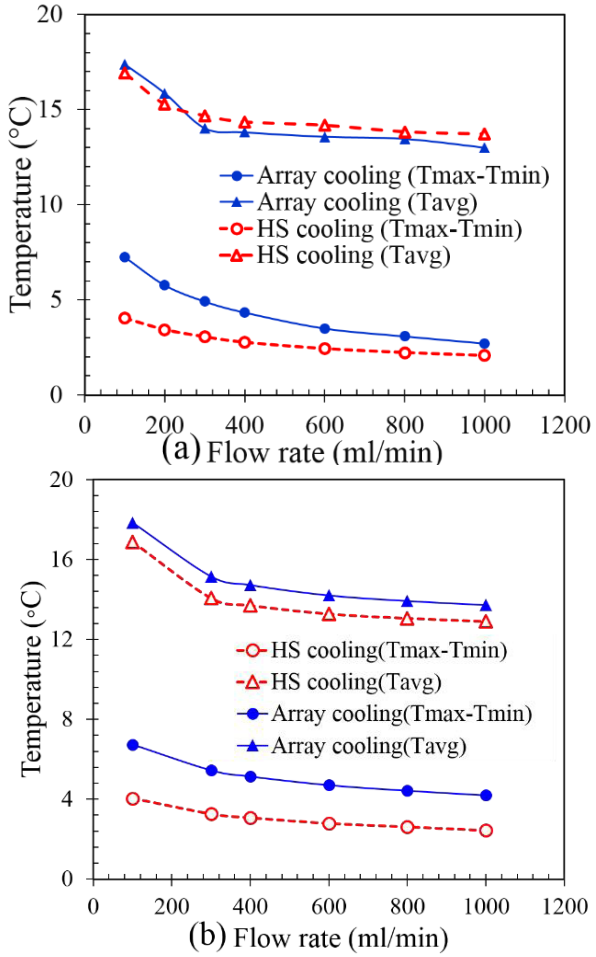

Fig. 18. Temperature uniformity comparison for hotspots cooling and uniform array cooling with (a) test case 1 and (b) test case 2 under different flow rates.

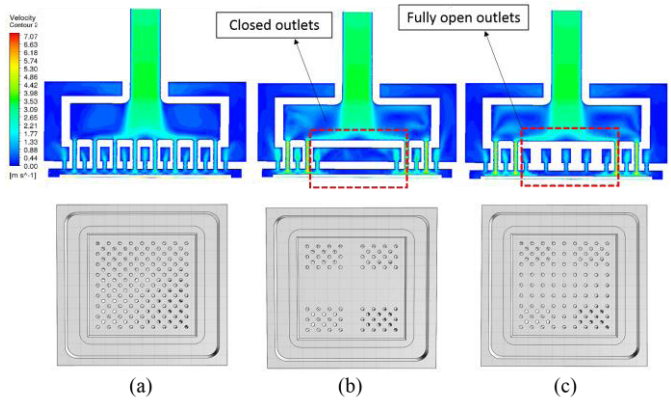

Fig. 19. Different configurations studied. (a) Uniform array cooling. (b) Hotspot targeted cooling with closed outlets for nonheating region. (c) Hotspot targeted cooling with fully open outlets (test case 1).

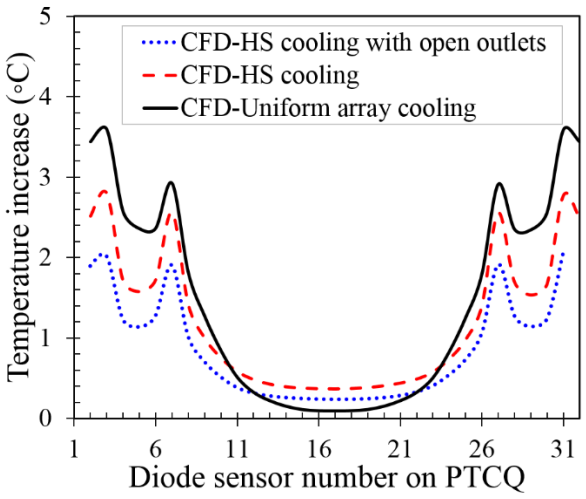

Fig. 20. Temperature profile for the three configurations for test case 1 (flow rate = 600 mL/min and $Q = 4.1$ W).

for test case 2 are shown for different flow rates in Fig. 17. It can be observed that for all flow rates, the peak temperature of the hotspots with uniform array cooling shown in Fig. 17(a) is more locally peaked than for the hotspot targeted cooling. Moreover, the peak temperature drops down significantly with hotspots target cooling as shown in Fig. 17(b), resulting in better temperature uniformity.

For a more detailed analysis, Fig. 18 shows the temperature difference and averaged temperature as a function of the flow rate for the two test cases. The temperature difference is defined as the difference between the maximum temperature and the minimum temperature. In general, it shows that the required flow rate for the hotspot targeted cooling is smaller compared with the full array cooler in order to achieve the same level of temperature uniformity. As shown in Fig. 18(a), for the same level of temperature uniformity with 3.8 °C, the required flow rate for hotspot targeted cooler is only 200 mL/min, which is three times lower than for the uniform array cooler. For test case 2 shown in Fig. 18(b), the required flow rate of the hotspot targeted cooler is about six times lower with the temperature uniformity of 4 °C. Furthermore, it can be observed that the average chip temperature is similar for both cooling solutions.

C. Nozzle Array Distribution Configurations

Hotspot targeted cooling with placing the inlet/outlet nozzles only at the hotspot regions shows good cooling performance and temperature uniformity. However, there is the possibility to place the outlet nozzles on the nonheater region to reduce the pressure drop. In Fig. 19, three different hotspots targeted cooling configurations are compared. Configuration 1 is the uniform nozzle array cooling, configuration 2 is the hotspot targeted cooling outlet present only next to the inlet nozzles, and configuration 3 is the hotspot targeted cooling with the outlet nozzle present across the whole chip surface. The CFD modeling results for the pressure drop for configuration 3 is 0.63 bar at a flow rate of 600 mL/min, which is 1.12× lower than configuration 2 with closed outlets in the nonheating region.

Moreover, the temperature profile for the three configurations is compared in Fig. 20. It can be seen that configurations 2 and 3 show lower peak temperature than configuration 1, and a higher temperature for nonheated region, which results in a lower temperature difference. This is due to the limited heat

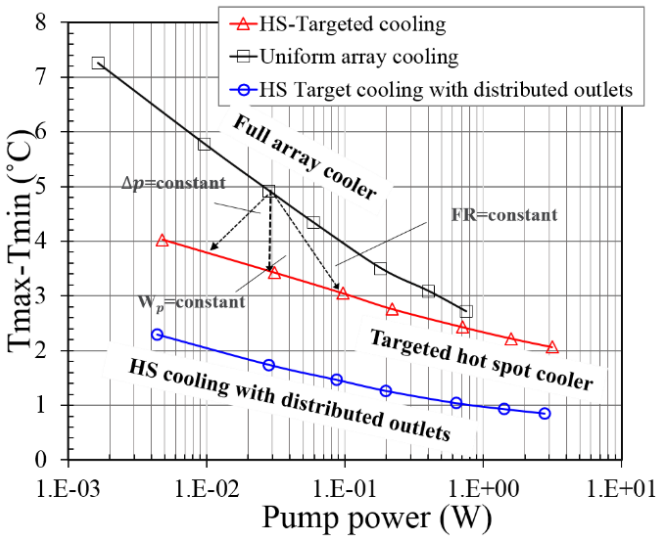

Fig. 21. Thermal/hydraulic tradeoff analysis for hotspots targeted cooling (test case 1).

TABLE II
THERMAL/HYDRAULIC TRADEOFF MODELING RESULTS (TEST CASE 1)

		$\dot{V}$ (ml/min)	ΔP (Bar)	$\dot{W}_p$ (W)	ΔT_{uni} (°C)	T_{avg} (°C)
Reference: full array cooling		600	0.18	0.18	3.5	13.5
$\dot{V}$ = C	DS2	600	0.7	0.71	2.4	14.1
	DS3	600	0.63	0.63	1.03	13.5
$\dot{\Delta}$p = C	DS2	275	0.18	0.082	3.04	14.6
	DS3	274	0.18	0.08	1.44	13.2
$\dot{W}_p$= C	DS2	370	0.29	0.18	2.8	14
	DS3	380	0.28	0.18	1.3	13.1

(notes: DS2: hotspot targeted cooling with locally closed outlets; DS3: hotspot targeted cooling with open outlets; C: constant value; •T_{uni} is defined as the difference between the maximum and minimum chip temperature)

spreading effects along the nonheater region. For configuration 3, it shows a lower peak temperature than configuration 2 and lower temperature in the nonheated areas but the smaller difference with lower pressure.

In Fig. 21, the comparison between the hotspot targeted cooler with configurations 2 and 3 and the full array cooler is shown. The performance of the three coolers is shown as a curve in terms of the temperature difference as a function of the required pumping power for a range of flow rates. In this benchmarking chart, a better cooler performance is indicated by a lower temperature difference and lower required pump power. The performance of the coolers is now compared for different constraints:

1) same pressure drop over the cooler;
2) same flow rate;
3) same pumping power.

As shown in Table II, for the same pressure drop of 0.18 bar, the chip temperature difference ΔT_{uni} reduces by a factor of 2.4 for the hotspot targeted cooler of configuration 3 compared with the full array cooler, and it requires two times less flow rate and pumping power. For the same flow rate of 600 mL/min, ΔT_{uni} reduces by a factor of 1.6, but it requires four times larger pressure drop; As for the same pumping power at 0.18 W, ΔT_{uni} drops by 63% compared with the full array cooler. In summary, the hotspot targeted cooling with open outlets in the nonheating regions is more energy-efficient compared with the other configurations, despite the higher pressure drop compared to the uniform array cooling. This indicates that the gain in thermal performance due to the targeted cooling by concentrating the liquid coolant at the high heat flux locations outweighs the detrimental impact of the increased required pressure drop and pumping power. Therefore, the hotspot targeted cooler outperforms the uniform array cooler in terms of energy efficiency. This modeling study provides a guideline for the outlet placement during the design of hotspot targeted cooling.

In this article, the nozzle diameter and the nozzle pitch have been fixed using the same values as the uniform case, as an illustration. An interesting step for us to further look into is the nozzle configurations with more flexible and optimized designs for the hotspots.

VI. CONCLUSION

In this article, a low-cost energy-efficient hotspot targeted cooling concept is introduced. The hotspot targeted cooler demonstrator is fabricated by polymer-based high-resolution SLA with nozzle diameters of 300 μm and a pitch of 1 mm using a water-resistant polymer material. The thermal and pressure drop performance of the demonstrators is characterized by using an advanced programmable thermal test chip and an accurate closed flow loop measurement system. The temperature measurements show a peak temperature reduction of 16% and 42% at a flow rate of 600 mL/min compared with the full array cooler for the targeted hotspot coolers of test cases 1 and 2, respectively, indicating that concentrating the liquid coolant on the locations where it is needed can result in a significant reduction of the chip peak temperature due to the locally increased coolant flow rate. On the other hand, the measured pressure drop of the hotspot targeted cooler for test case 1 is 3.2 times higher than the uniform array cooling, while the pressure drop for test case 2 is 5.9 times larger.

The detailed conjugate heat transfer CFD models have been used to assess the local flow distribution and temperature uniformity for the different coolers. The modeling results have been successfully validated, showing good agreement with the temperature and pressure measurements. The modeling results show that the expected local cooling rate for the hotspot targeted cooling is $m^{0.67}$ times higher than the average cooling rate for the full array cooler, where m is defined as the ratio between the number of inlet nozzles in the full array cooler and in the hotspot targeted cooler. As a result, the hotspot target cooler requires a lower flow rate to achieve the same level of the temperature uniformity compared with the full array cooler. However, the expected pressure drop for the hotspot targeted cooler is m^2 times higher than the uniform array cooling.

A detailed tradeoff between the thermal performance improvements and the higher required pressure drop and pumping power shows that the hotspot targeted cooler outperforms the uniform array cooler in terms of energy efficiency despite the increase in pressure drop. This higher performance is observed for three different bases for comparison: constant flow rate, constant pressure drop, and constant pumping power.

The validated CFD models also show that the hotspot targeted cooler can be further improved by providing outlet nozzles over the full chip area instead of near the inlet nozzles covering the hotspot areas only. The implementation with the additional outlet nozzles achieves a further reduction of the pressure drop across the cooler by 12% and a reduction of the maximum temperature difference by a factor of 2, resulting in an even more energy-efficient design.

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