Feasibility Design of Tight Integration of Low Inductance SiC Power Module with Microchannel Cooler

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***Abstract*—Traditional power module packaging becomes a limiting factor to fully exploit the benefits offered by high speed and high-temperature silicon carbide (SiC) devices. Especially in the automotive applications, the parasitic oscillation and localized hot spots have become unneglected problems. In this paper, an ultra-low inductance wire bondless power module with an integrated microchannel cooler is proposed. Flip-chip bonding with solder balls is used to replace traditional wire bonds to realize ultra-low inductance paths for both power- and gate-loop connections. As a result, the parasitic inductance of the proposed 1200 V, 300 A half-bridge SiC power module can be reduced to 0.93 nH. Then, to achieve high power density, an advanced low thermal resistance packaging architecture with an integrated microchannel cooler is proposed. Through femtosecond laser etching of the microchannels into the power module DBC ceramic layer, the microchannel cooler can be tightly embedded into the power module, resulting in a very high cooling capability. This method drives the module junction-to-coolant thermal resistance down to 0.073 $cm^2 \cdot K/W$, which leads to approximately 65% reduction of thermal resistance compared with the conventional cooling integration structure. Moreover, a corresponding fabrication process is developed to enable the tight integration of the microchannel cooler structure.**

Keywords—SiC power module, low parasitic inductance, integration, microchannel cooling

I. INTRODUCTION

High power density is one of the ultimate goals for power electronic converters in electric vehicle applications. SiC devices have been proven to be capable of high frequency, high-temperature, and high-voltage characteristics, which are key enablers in the evolution of electric vehicle technologies [1]. However, these benefits come at the cost of significant challenges for power module packages [2]. For example, SiC devices are highly sensitive to the parasitic inductance of module packages because of the fast switching speeds. They will lead to high voltage overshoot and parasitic oscillations [3]. Moreover, due to the increased operating temperature, improvement of cooling capability is also a key aspect for SiC power modules. Therefore, to fully realize the benefit offered by the high speed and high-temperature SiC devices, it is very important to develop advanced power module packaging architectures with low parasitics and high cooling capability.

Recent studies have pointed out that bond wires and Direct-Bonded-Copper (DBC) substrate copper traces are the major sources of module parasitic inductance and account for nearly 50% of the total module commutation-loop inductance [4]. Therefore, eliminating bond wires and optimizing the DBC substrate layout can lead to lower parasitic inductance. In [5], low parasitic wire-bonded power modules are built by applying the P-cell and N-cell concepts, resulting in power module inductances of 6.5 nH and 4.8 nH, respectively. In [6], a 5 nH wire-bonded power module is realized by utilizing a power overlay and laminated busbar connections. In [7], a flexible printed circuit board (FPCB) based SiC power module with 3D integration structure was proposed. Benefitting from the flexibility of PCB and thin PCB substrate, the optimized power loop inductance is 0.79 nH. In [8], solder ball array interconnector was utilized to replace bond wires, which optimizes interconnection parasitic inductance to under 1 nH. Thus, wire bondless chip topside interconnect technologies are the most attractive packaging solutions for an ultra-low parasitic inductance power module.

To address the thermal challenges raised by improving power density in electric vehicle applications, some novel cooling methods such as spray cooling, jet impingement cooling and microchannel cooling have been presented [9]. However, the cooling capability of the spray and jet cooling are still limited by the thermal resistance of the DBC substrate and baseplate. Moreover, integration of spray and jet cooling

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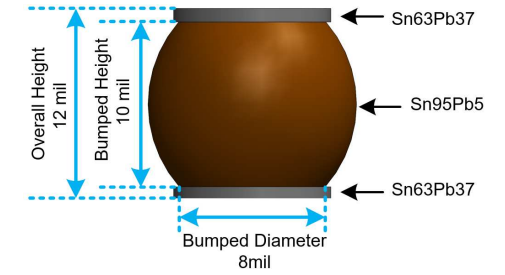
requires complex structures that can increase the cooler size [10]. Integration of a microchannel cooler into the power module DBC ceramic layer reduces the junction-to-coolant thermal resistance and improves the cooling capability simultaneously. In addition, etching the microchannel inside the DBC layer can also increase the cooling surface area, resulting in a high cooling capability. Embedded microchannels with 3D manifold heat sink coolers (EMMCs) show great potential to reduce the pressure loss and improve the thermal performance. K. W. Jung investigated thermal design considerations and constraints for developing an embedded silicon/SiC microchannel cooling with 3D manifold architecture capable of removing up to 1 kW/cm^2 utilizing single/two-phase flow and heat transfer schemes [11]. With high efficiency 3D manifold embedded microchannel cooling integrated into the DBC layer, the power converter can achieve much higher power density, while maintaining a safe operation temperature.

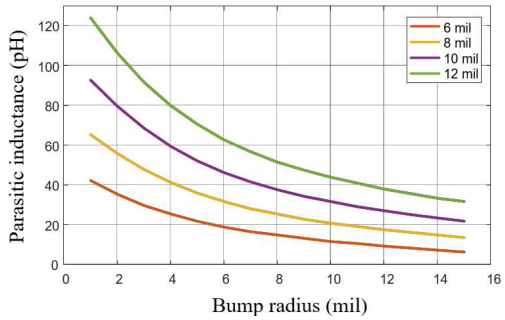
In this paper, a wire bondless and highly integrated power module architecture with an embedded microchannel cooler is proposed to realize ultra-low parasitic inductance and high cooling capability. The paper's organization is shown as follows: In the first section, a solder ball connection structure and low inductance power module structure are proposed. In the second section, the fabrication flow of power module was introduced. In the third section, the fabrication process of the embedded microchannel cooler and low thermal resistance integration structure are analyzed.

II. LOW INDUCTANCE POWER MODULE DESIGN

The reduction of power module parasitic inductance is realized by the combination of a wire bondless chip topside connection method and an optimized commutation-loop architecture. At first, a solder-ball array is applied to replace the traditional wire bonding to minimize the chip connection inductance in the power module. The parasitic inductance of a single solder ball is determined by bump radius and height. The typical geometric structure of a solder ball includes two flat cylinders and one flattened sphere, as shown in Fig. 1 (a). The parasitic inductance of different solder ball sizes was extracted from ANSYS Q3D simulations, as Fig. 1 (b) shows. Parasitic inductance decreases with solder ball height and bump radius. With consideration for the manufacturing process and the power module overall height (insulation demands), 10-mil bump height solder balls were selected.



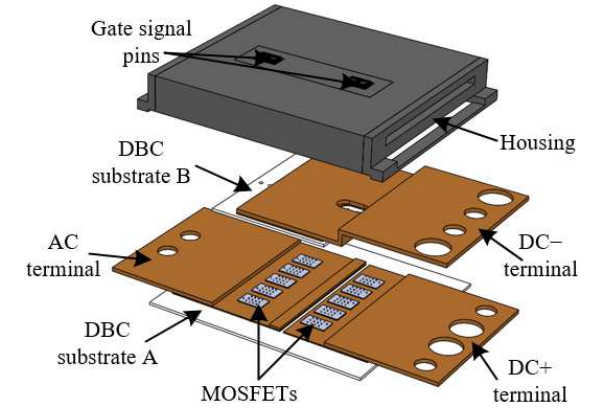
(a) Solder ball geometric model



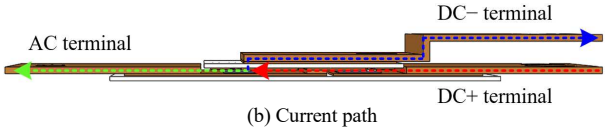
(b) Parasitic inductance at different bump radius and height

Fig. 1. Solder ball geometric model (a) and parasitic inductance simulation results (b).

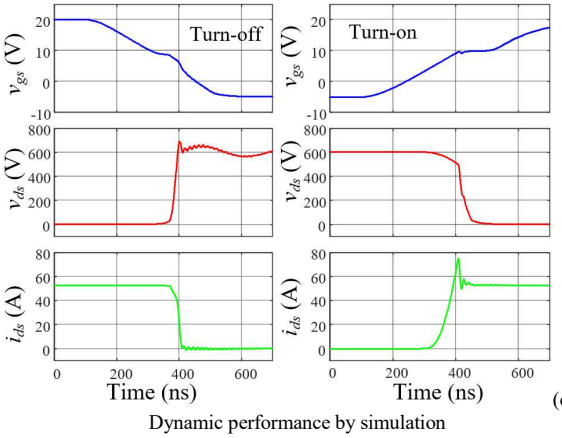
Benefitting from the solder balls chip topside interconnect method, further, a 2.5D solder ball sandwich concept is developed as the power module commutation-loop structure, as shown in Fig. 2 (a). With this 2.5D sandwich architecture, the magnetic field cancellation effect between the DC+ path and DC- path can be maximized. To minimize the total thermal resistance, the SiC chips were mounted on the top copper layer of substrate A while the microchannels are etched into the



(a) Power module structure



(b) Current path



(c) Dynamic performance by simulation

Fig. 2. Proposed power module structure and its dynamic performance.

bottom of the DBC substrate A. The DC+ terminal and DC− terminal were laminated tightly to minimize the commutation loop inductance. The gate signal pins were directly plugged into DBC substrate B to minimize its gate loop inductance. The current path inside the power module to achieve significant mutual inductance cancellation of the commutation loop was shown in Fig. 2 (b). By optimizing the chip connection and commutation loop, the parasitic inductance can be reduced to 0.93 nH at 10 MHz. The parasitics of the power module were extracted by ANSYS Q3D and utilized in circuit simulations in LTspice to investigate the power module dynamic performance as shown in Fig. 2 (c). The overshoot voltage during the turn-off process is only 92 V at DC bus voltage of 600 V.

III. Power Module Fabrication Process

The fabrication process of the power module is shown in Fig. 3, including three reflow soldering processes. First of all, the substrate A copper pattern was developed by chemical etching and microchannels were developed by laser etching into substrate A's AlN ceramic layer. Then, Au80Sn20 solder balls were bumped onto the electroless nickel-plated SiC MOSFET chip source and gate pads. The first reflow process was to attach solder balls bumped MOSFETs chips and DC+ terminal and AC terminal onto substrate A. In the next step, substrate B's copper pattern was also developed by chemical etching and through holes were laser-drilled. Filling through holes by sintered silver guarantees high thermal conductivity, high reliability and low resistivity performance. The DC− terminal and gate signal pins were attached to substrate B during the second soldering process. The third soldering process was to attach substrate A and substrate B. Next, the 3D printed high-temperature housing was applied and epoxy resin was coated to improve the insulation strength inside the power module. The final step was to attach the lid to the power module housing to seal the coated encapsulant.

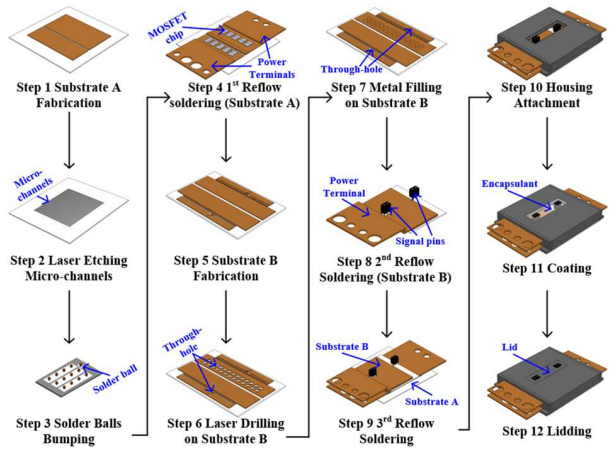
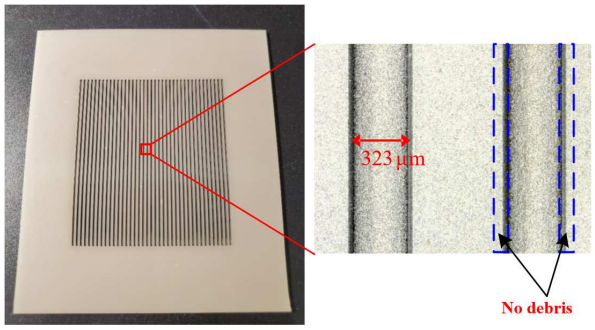


Fig. 3. Fabrication flow chart.

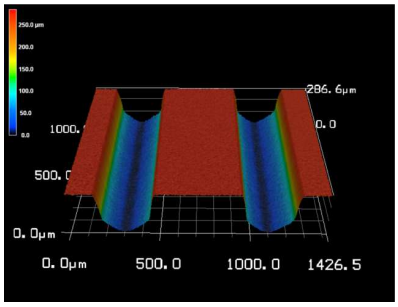
IV. Microchannel Cooler Fabrication and Integration

The proposed 3D manifold microchannel cooler consists of two main components: manifold and microchannels. The microchannels with convective liquid cooling are used to extract the heat from the power sources. The 3D manifold with multiple inlet and outlet ports is bonded on top of the microchannels, which can deliver the liquid coolant through the DBC microchannels. The proposed integrated structure can reduce the fluid length and therefore reduce the pressure drop.

A DBC substrate with a 304 μm copper layer and a 635 μm AlN layer was chosen to build the microchannel structure. Since AlN is a brittle material, high precision femtosecond laser etching was utilized. As shown in Fig. 4 (a), the DBC microchannels with channel width of 323 μm and a channel depth of 273 μm were etched inside the copper layer, with no process debris observed around the cutting surface. The surface roughness and etched channel topology are evaluated as illustrated in Fig. 4 (b).



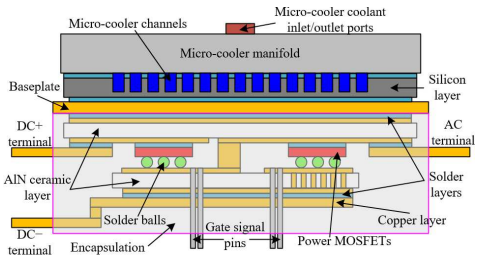
(a) Femtosecond laser etching of microchannels without debris



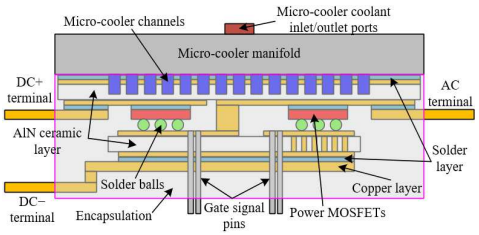
(b) Laser scanning microscopy image of microchannels

Fig. 4. Femtosecond laser etching of microchannels.

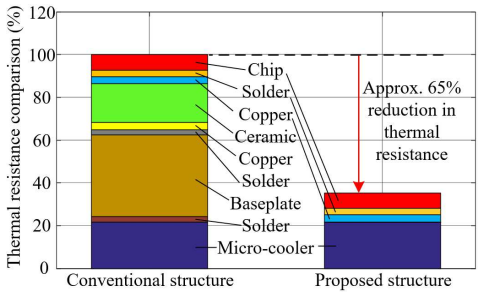
The integration structure of the microchannel cooler with the wire bondless power module is shown in Fig. 5 (b). The 3D manifold was bonded to the DBC AlN layer with no leakage of fluid between the microchannels, which guarantees the cooling performance of microchannel cooler. By eliminating the baseplate layer, DBC bottom copper layer and two solder layers between the micro-channel cooler and DBC ceramic layer, the junction-to-coolant thermal resistance achieved is 0.073 $cm^2 \cdot K/W$. Compared with the conventional integration structure in Fig. 5 (a), the thermal resistance is reduced by approximately 65% as shown in Fig. 5 (c).



(a) Femtosecond laser etching of microchannels without debris



(b) Laser scanning microscopy image of microchannels



(c) Laser scanning microscopy image of microchannels

Fig. 5. Femtosecond laser etching of microchannels.

V. Conclusion and Future Work

In this paper, an ultra-low inductance wire bondless power module with an integrated microchannel cooler is proposed. The parasitic inductance of a half-bridge SiC power module was reduced to 0.93 nH by introducing the ultra-low inductance solder ball structure. The microchannel cooler was integrated tightly into the power module with a junction-to-coolant thermal resistance of 0.073 $cm^2 \cdot K/W$. Compared with the conventional cooling integration structure, the junction-to-coolant thermal resistance can be reduced by approximately 65%.

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