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Research Paper

Experimental characterization and model validation of liquid jet impingement cooling using a high spatial resolution and programmable thermal test chip

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HIGHLIGHTS

- A high spatial resolution and programmable thermal test chip is introduced.
- A high level detail of local heater structures is necessary for high heat removal rates of multi-jet cooling during CFD modeling analysis.
- Thermal performance benchmarking between the single jet cooling and multi-jet cooling for electronic applications.
- Correlations development for single jet cooling and multi-jet cooling with locally distributed outlets configurations.

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ABSTRACT

High efficiency direct liquid jet impingement cooling with locally distributed outlets is very promising in high power electronic devices. In order to elucidate the flow-thermal interaction for micro-scale jet impingement cooling, sensitive temperature measurements with high spatial and temporal resolution are required. In this work, a programmable thermal test chip with 832 heater cells with 75% heater uniformity and 32 × 32 array of temperature sensors is introduced. The detailed measured temperature maps for different power dissipation patterns allow the in-depth study of the thermal performance of liquid jet impingement coolers and the detailed experimental validation of complex CFD models. The modeling and measurement study is applied to two jet impingement cooling implementations: (1) a single jet cooler with a 2 mm diameter nozzle, and (2) a multi-jet cooler with a 4 × 4 array of 500 μm inlet nozzles and distributed outlet nozzles. For both cooler configurations, the temperature measurements and CFD modeling results are investigated and compared for uniform and hot spot power dissipation patterns.

1. Introduction

Direct liquid jet impingement cooling [1] is an efficient cooling technique for high power electronics that has been successfully applied with various materials including Si [2], ceramic [3], metal [4] and plastics [5]. Bare die jet impingement cooling avoids the use of a thermal interface material (TIM), since the coolant is direct contact with the chip. In literature, detailed reports cover experimental, theoretical and numerical analyses of different impingement jet configurations. These configurations range from single submerged jet [5], to multiple submerged jets [6], and impinging jet cooling of electronic modules [7,8], configurations with common return [6] and with distributed returns [8]. However, limited experimental studies focus on chip level impingement jet cooling with locally distributed outlets due to the complicated internal cooler structures with sub-mm dimensions. Since impingement cooling can achieve high heat transfer coefficients, accurate experimental studies with high spatial and temporal resolution are required to capture the local thermal impact of the cooling. The experimental characterization of jet impingement involves both the study of the flow behavior through visualization, as well as the heat transfer between the heated chip and the impinging coolant. The focus of this paper is on the experimental characterization of the heat transfer.

The experimental study of jet impingement as an electronics cooling

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solution typically involves two key elements: (1) the heat source to create a constant heat flux, and (2) the temperature measurement technique. For the characterization of the fundamental heat transfer phenomena, uniform heating in the surface is most appropriate since other effects such as thermal spreading in the silicon are minimized. In the real application, however, the heated chip has non-uniform hot spots with peak heat fluxes up to 1000 W/cm^2 over very small areas (< 0.25 mm^2) [9]. The measurements can either be performed in a mock-up apparatus of the integration of the cooling solution or using a more realistic test vehicle with integrated heaters and temperature sensors, where each approach has its advantages and drawbacks. Heating elements in the mock-up include film heaters [10], thin metal sheets [11], platinum serpentine heaters [12], Cu blocks [13] or coated heaters [14] in Incomel or stainless steel meshes on the heat transfer surface. The drawbacks of these additional heater materials are the introduction of additional thermal interfaces in the measurement structure, which can affect the temperature distribution, and the change in surface in case the heaters are deposited on the surface, which will impact both the flow behavior and the heat transfer [14]. The temperature measurement methods can typically be categorized into optical and electrical techniques. The optical techniques can produce the temperature map of the heat exchanging surface without making contact, and thus without disturbing the measurement. These techniques require however visual access to the surface which limits the integration options for the test structure. Examples of these optical techniques include thermochromic liquid crystals (TLC) [24], temperature sensitive paint (TSP) [26] and infrared thermography [25]. Electrical measurement techniques on the other hand require physical contact (resulting in an additional contact resistance and disturbance of the measurements [20]) to measure the temperature at the limited number of discrete locations of the sensors. Thermocouples are a commonly used method which are placed on or near the heated surface that is being cooled by impinging jets [15–18]. An example is the study by Maddox [19] where an array of twelve K-type thermocouples embedded in the measurement block with a pitch of 3 mm was used to capture the temperature and heat transfer coefficient peak. Other temperature sensors are resistance temperature detectors (RTDs), which can be deposited on the heater surface as RTD film or integrated separately with the heat source [21–23], and thermistors which are very sensitive (up to 100 times more than RTDs and 1000 times more than thermocouples) by measuring the change in resistance with temperature. However, thermistors have self-heating problems and have a slow response for transient thermal measurements.

Alternatively, thermal test chips or thermal test vehicles with integrated heaters and sensors can be used for steady-state and transient thermal measurements in real application conditions, including all realistic interfaces. The on-chip integrated temperature sensors can be metal resistors, RTDs or diodes, while the integrated heaters can be polysilicon heaters, transistors and metal resistors to create either a uniform power dissipation or a predefined hot spots pattern. The drawbacks of the test vehicles are the higher cost and the required processing or packaging to be used in the test set-up. These test vehicles can be fabricated using simplified processing of metal heaters and RTDs on Pyrex [30] or full CMOS Si processing. In literature, only a small number of experimental studies using thermal test chips for liquid jet impingement cooling are available. Evelyn N. Wang et al. [27] used a 1 cm^2 Si thermal test chip with seven calibrated temperature sensors to study the performance of the microjet heat sinks, but the test chip used in the experimental investigations has a low spatial resolution. Richard et al. [28] carried out thermal experiments for a flat spray cooling system with nozzles angled to the surface of a silicon chip using only four micro-heaters for delivering peak heat fluxes and 29 RTDs. However, the spatial resolution of the temperature measurement is limited by the number of RTD temperature sensors. Especially in the case of hot spots cooling measurements, a higher spatial resolution is required.

In this work, a thermal test chip with high spatial resolution and a programmable power dissipation map is used for the thermal characterization of liquid jet impingement coolers with distributed returns. First, the features of the test chip, the design of the single jet and multi-jet impingement coolers and the experimental set-up are introduced. Next, the temperature measurements and CFD modeling of the coolers are investigated and compared for uniform and hot spot power dissipation patterns. Finally, the thermal performance for different outlet nozzle configurations is investigated using the validated CFD models for hot spot arrays.

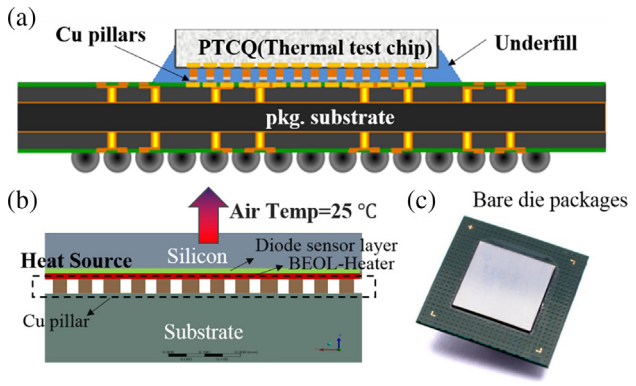

Fig. 1. Details of the thermal test chip: (a) cross section view of the PTCQ package; (b) schematic of the heater and diode temperature sensor layer; (c) photograph of the bare die package.

2. Experimental set-up

2.1. Advanced thermal test chip

In this study, a dedicated CMOS thermal test chip, named PTCQ (Packaging Test Chip Version Q) shown in Fig. 1(c) is used to characterize the temperature response of liquid jet impingement cooling. This 8 × 8 mm^2 test chip includes integrated heaters to program a custom power map and integrated sensors to measure the full temperature distribution map. As shown in Fig. 1(a), the entire PTCQ package includes the thermal test chip, the Cu pillars and underfill material, the package substrate, the solder balls and the PCB. The dimensions and material properties are listed in Table 1. Moreover, the integrated diode temperature sensor layer and heater cell layer are illustrated in Fig. 1(b). The size of the single diode temperature sensor is about 4.8 μm × 2.6 μm, which was fabricated using front-end of line (FEOL) semiconductor processing technology. Different from the temperature sensors, the heater cells were fabricated using back-end of line (BEOL) as resistors.

The test chip is divided into a 32 × 32 array of 240 × 240 μm^2 square cells with additional peripheral circuits with I/O and control cells in the central cross of the chip. The total number of the temperature sensor cells is 1024, marked with yellow[1] color shown in Fig. 2(a). All these cells contain a diode in the center of the cell as temperature sensor, resulting in a detailed temperature map measurement with 32 × 32 'thermal pixels' across the die surface. The voltage drop across the diode for a constant current is used as the temperature sensitive parameter of the sensor. The 95% confidence interval of the calibrated sensitivity is −1.55 ± 0.02 mV/°C for a current of 5 μA in the temperature range between 10 and 75 °C. This current level is sufficiently high to ensure stable operation of the diode as temperature sensor while it maintains the intrinsic power dissipation at a low level of 4 μW preventing it from self-heating.

[1] For interpretation of color in Fig. 2, the reader is referred to the web version of this article.

Table 1
Dimensions and Material properties.

Layer (from top)	Dimensions (mm × mm × mm)	k or k_x, k_y, k_z (W/m-K)
Silicon die	8 × 8 × 0.2	150
BEOL	8 × 8 × 0.002	0.25 × 0.25 × 0.5
Cu pillars and underfill	8 × 8 × 0.1	0.4 × 0.4 × 8
Substrate	14 × 14 × 0.33	10 × 10 × 0.6
PCB	35 × 35 × 0.6	12 × 12 × 0.6

defined by nozzle to chip distance H. The inlet diameter is defined as d_i while d_o is used for the outlet diameter. The nozzle plate thickness is regarded as t. The jet-to-jet pitch is given by L.

In this section, two types of impingement jet coolers have been assembled onto the PTCQ thermal test chip package: (1) a single jet cooler with one inlet nozzle and 6 outlet nozzles shown in Figs. 4, and 2) a multi-jet cooler with a 4 × 4 array of inlet nozzles shown in Fig. 5. The single jet cooler demonstrator is fabricated in plexiglass with inlet and outlet tube diameters of 6 mm. The diameter of the inlet nozzle on top of chip surface is 2 mm. The final assembly of the single jet cooler

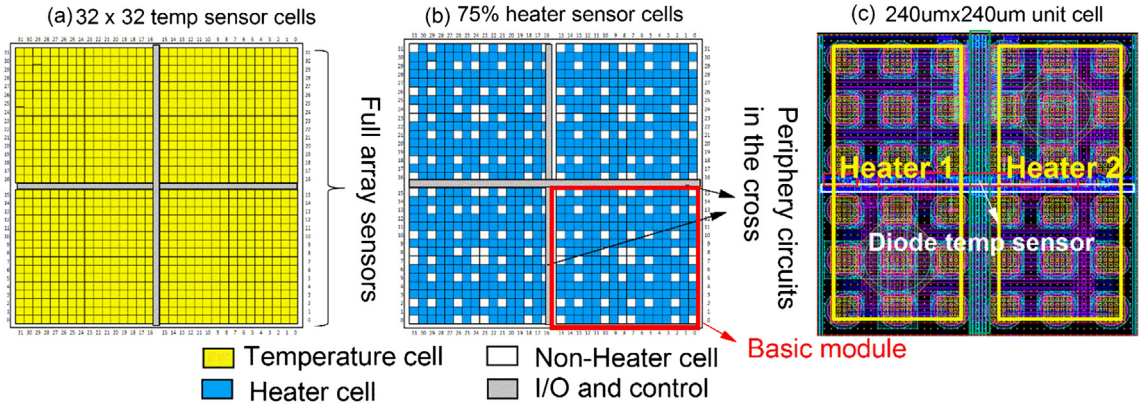

Fig. 2. Floorplan of the 8 × 8 mm^2 PTCQ thermal test chip: (a) configurations of 32 × 32 array of temperature sensors; a) configurations of 832 programmable heater cells; (c) details of the metal meander heaters within one cell (240 × 240 μm^2).

As shown in Fig. 2(b), the blue square elements represent the heater cells while white square elements stand for non-heater cells. Therefore, there are 832 cells indicated as 'heater cells' within the 32 × 32 array. The single heater cell is equipped with two 200 × 100 μm^2 metal meander heaters in the back-end of line (BEOL) shown in Fig. 2(c). The maximal power dissipation of each cell is 100 mW for a voltage of 1 V. The calibrated resistance per heater cell is 10 Ohm. Including the periphery circuits with 192 grey square elements, the "heater cells" covers 75% of the chip area (832/1089 = 75%). Each of those cells is individually controlled by a local switch, resulting in a custom power map on the test chip ranging from quasi-uniform power dissipation with 75% coverage to localized hot spots. The other cells marked with white color in the test chip contain a variety of mechanical stress sensors. These stress sensors on the chip have been measured in our previous studies to evaluate the induced stress in the chip during the die stacking [29] and the chip packaging process [31]. Moreover, the stress caused by local hot spot power dissipation [32] has been also investigated by these stress sensors.

In order to supply the current to the test chip and to read out the data, the test chip needs to be packaged, as discussed in [33]. To apply the test chip for the thermal evaluation of jet impingement cooling, the test chip is packaged face-down in a 14 × 14 mm^2 flip chip ball grid array package (FC-LPBGA). In the bare die package, the backside of the Si chip is exposed allowing direct contact of the liquid coolant to the heated chip.

2.2. Chip level impingement jet cooler concepts

Fig. 3 illustrates the critical parameters in the cross section of a generic impingement jet cooler with locally distributed outlets in between the inlet nozzles. Three different levels are shown in the cooler schematic Fig. 3(b): the inlet plenum level, the outlet plenum level and the impingement jet cooling level (cavity level). The inlet plenum is the flow distributor which can feed the liquid coolant for all inlet nozzles. The outlet plenum is the collector which can collect the liquid for drainage. The impingement cooling happens in the cavity region on thermal test chip as well as the outside tube connections are shown in Fig. 4(a). Fig. 4(b) shows the cross-section view of the single jet cooler indicating the placement of the individual parts, including part 1, part 2 and the O-ring. The cooler is assembled on the organic package substrate. Fig. 4(c) and (d) show the details of the arrangement of the single inlet and six outlets. The objective of this demonstrator is to capture the temperature distribution of the liquid impinging jet on the heated surface in detail.

The 4 × 4 array cooler is fabricated in PVC (polyvinyl chloride) with 500 μm diameter inlet and outlet nozzle diameters. More details on the cooler design and fabrication can be found in [8]. Fig. 5(a) shows the assembly of the different parts on the PTCQ package and the PCB. The exploded view shows the critical parts with the nozzle plate and the inlet/outlet divider. The exact placement of the nozzle plate is also shown in Fig. 5(b). The objective of this cooler is to evaluate the jet-jet interactions and the hot spot targeted cooling performance. The two types of coolers are assembled on the PCB board shown in Fig. 5(c), which is connected to the data acquisition system. The voltage of the sensors can be measured to extract the temperature value.

The geometry parameters of the single jet cooler and the multi-jet cooler are both summarized in Table 2. In this experimental set-up, a copper tube is used to connect the cooler to the flow loop system. Since the outer diameter of the copper tube is 6 mm, the designed diameter for both the inlet tube $D_{i\text{-}tube}$ and outlet tube $D_{o\text{-}tube}$ is also 6 mm.

2.3. Experimental set-up

Fig. 6 shows the dedicated experimental test set-up for the accurate flow and pressure measurements in the cooler and the temperature measurements in the test chip. All the sensors in the set-up are connected to and controlled by LabVIEW, allowing operation of the flow loop either in a controlled mass flow rate mode or a controlled pressure mode. The flow loop contains a magnetically coupled gear pump with a maximum flow rate of 3 kg/min and a maximum pressure of 11.5 bar, a mini Cori-FLOW mass flow meter with a range of 0.1–3 kg/min and an accuracy of ± 0.2% as a percentage of reading (RD), and a particle filter

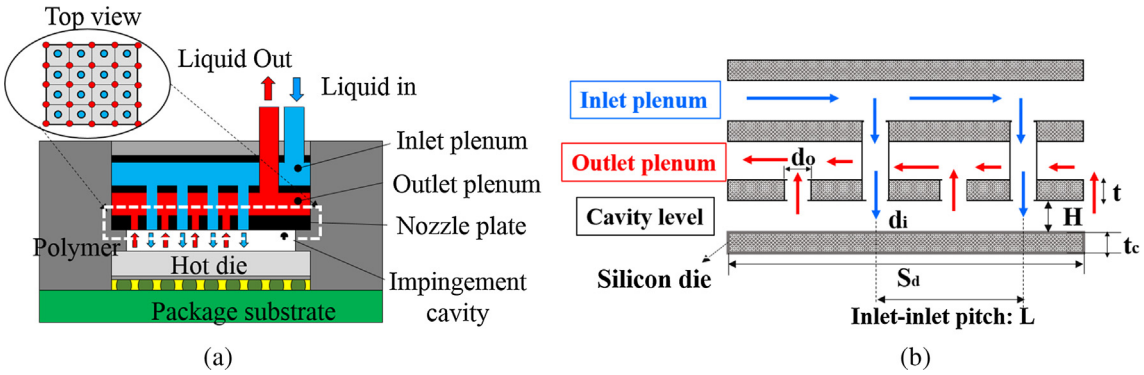

Fig. 3. Chip level impingement jet cooler: (a) generic impingement cooler cross section; (b) schematic with geometry parameters.

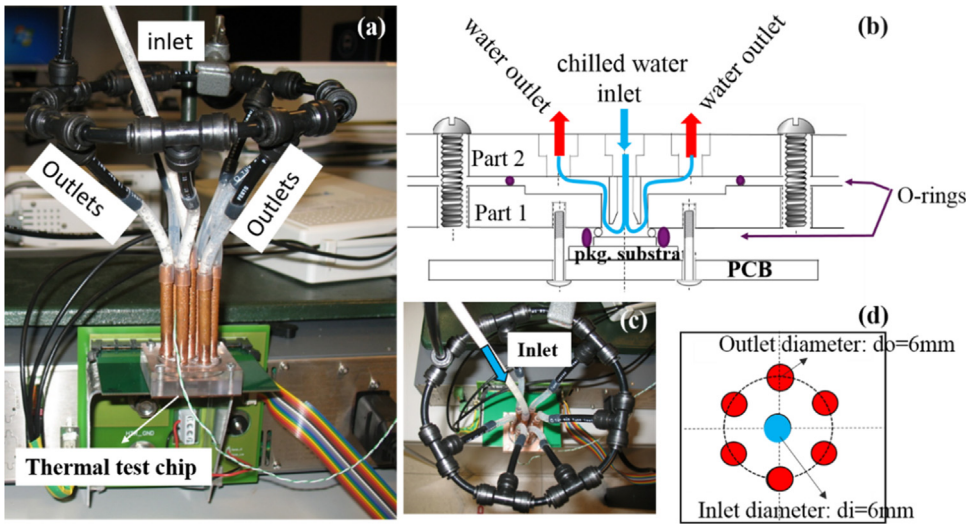

Fig. 4. Demonstration of the chip level single impingement jet cooler: (a) experimental set-up photo of single jet cooler; (b) schematic view of the cooler with different parts; (c) and (d) photo and isometric drawing of single inlet and six outlets.

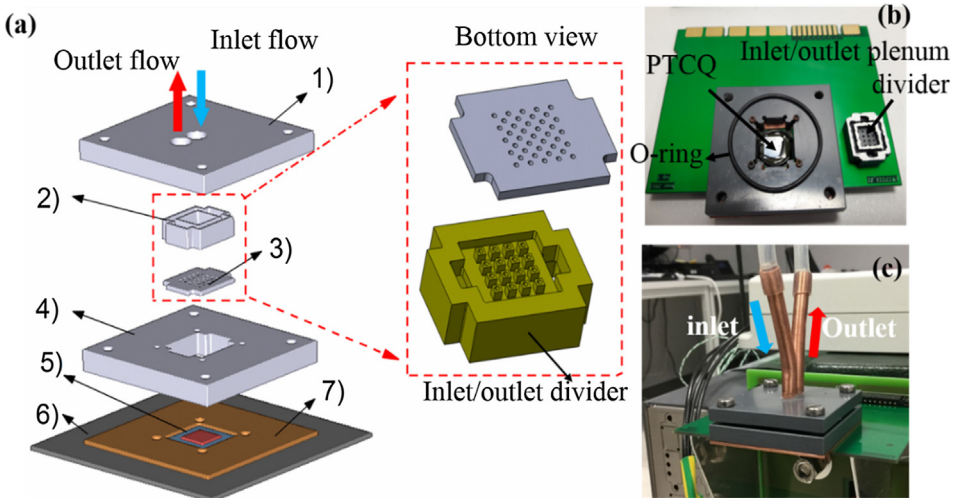

Fig. 5. Demonstration of the chip level 4 × 4 impingement jet cooler: (a) CAD design details of different individual parts; (b) photo with the arrangement of nozzle placement; (c) final assembly of 4 × 4 impingement jet cooler. (1-Cover layer, 2-inlet/outlet plenum, 3-nozzle plate, 4-support structure, 5-PTCQ thermal test chip. 6-PCB, 7-copper spacer).

with a mesh size of 25 μm. A differential pressure gauge (EL-PRESS) is used to measure the pressure drop across the cooler with an accuracy of ± 0.5% FS in the range between 0.2 and 5 bar. Thermocouples with an accuracy of 2.2 °C are used to measure the coolant temperature before and after the cooler. The 95% confidence interval of the calibrated sensitivity of the temperature sensor on the test chip is −1.55 ± 0.02 mV/°C for a current of 5 μA in the temperature range between 10 and 75 °C. The measurement uncertainty for the sensor and heater voltage are 1 mV and 1.6 mV respectively. The chip temperature sensors allow absolute temperature measurements with an accuracy of ± 2–3 °C.

A liquid-liquid heat exchanger is used to cool the coolant back to the set-point of 10 °C. In this work, DI-water is used as the coolant during the tests, with specified temperature at 10 °C and ambient temperature is kept at 25 ± 1 °C. The experimental conditions are summarized in Table 3. During the measurement, the chilled water set with 10 °C was

Table 2
Geometry parameters comparison.

Parameters	Single jet	Multi-jet
N×N	1	4 × 4
$D_{i\text{-}tube}/D_{o\text{-}tube}$	6 mm/6 mm	6 mm/ 6 mm
d_i	2 mm	500 μm
d_o	Common outlet	500 μm
H	2 mm	300 μm
t	7 mm	1 mm
t_c	0.2 mm	0.2 mm
L	8 mm	2 mm

applied to the cooling system without turning on the heater cells. After waiting 30 min, the steady-state chip surface temperature distribution was extracted by measuring the voltage across the 32 × 32 array of diode sensors. After that, the heaters with programmable pattern were turned on a waiting time of 30 min was used to achieve the steady-state regime. Finally, the temperature distribution map of the thermal test chip was measured.

3. Numerical modeling and evaluated thermal metrics

3.1. Numerical modeling

In order to investigate the hydraulic and thermal phenomena in the cooler numerically, conjugated heat transfer computational fluid dynamic (CFD) models have been created in Ansys-Fluent for both the single jet and the multi-jet cooler shown in Fig. 7.

These simulations include the conduction and convection in the fluid domain for the coolant as well as the conduction in the solid domain. The solid domain includes the test chip, whereas the thermal impact of the Cu pillars and underfill material, the package substrate, the solder balls and the PCB is represented by an equivalent convective boundary condition. The model dimensions are summarized in Table 1. The first layer thickness of the boundary layers is 1 μm, which is calculated from the Y plus number ($Y^+ < 1$). The maximum boundary layer number is set as 20 with a growth rate of 1.2. As shown in Table 4, the Richardson extrapolation for the discretization error is 0.3% for the stagnation temperature of the single jet cooler. Based on the meshing sensitivity study, the number of elements for the full models is 2.5 million and 5.9 million for the single jet and multi-jet model

Table 3
Experimental conditions.

Experimental conditions	Single jet cooler	4 × 4 multi-jet cooler
Inlet temperature	10 °C	10 °C
Chip power	24 W	50 W
Heat loss	0.35 W	0.6 W
Flow rate	200, 300, 600 ml/min	300, 600 ml/min

respectively. The heat flux boundary condition is applied to the locations that correspond to the activated heater cells in the test chip. All the boundary walls are set as adiabatic wall since the cooler material is plastic with low thermal conductivity. The inlet temperature is set to 10 °C. A velocity boundary condition is given at the top inlet feeding tube for flow rates between 200 and 600 ml/min. The boundary condition for the outlets is set as 'pressure out'. Based on this region, the RANS-based turbulent model is chosen as transition SST model which can capture the laminar flow and transition flow [1]. The "SIMPLE" algorithm is used as the solution method. The numerical scheme used in the simulation is QUICK scheme. The convergence criteria were set at $1e^{-5}$ for continuity, $1e^{-6}$ for energy and $1e^{-6}$ for *k*, ω and momentum (x, y and z components of velocity), respectively. For all the simulations, the net imbalance of overall mass, momentum and energy is kept below 0.02%.

3.2. Thermal metrics definitions

This section describes the full chip temperature map measurements with the quasi-uniform power dissipation and hot spots patterns, shown in Fig. 1, for the fabricated coolers. The overall thermal performance of the cooler is expressed in terms of the thermal resistance defined as follows:

$$R = (T_h - T_{in})/(Q_{heater}) \quad (1)$$

where T_h is the local chip temperature, T_{in} is the coolant inlet temperature and Q_{heater} is the heat generated in the heater cells based on the measured electrical current and heater voltage. This thermal performance estimation of the assembled cooling solution also includes the heat losses through the cooler material into the ambient and the heat losses through the bottom side of the assembled test board. Based on the measurement uncertainty analysis, the analysis of the propagated measurement uncertainty results in a value of ± 1.8% for the reported

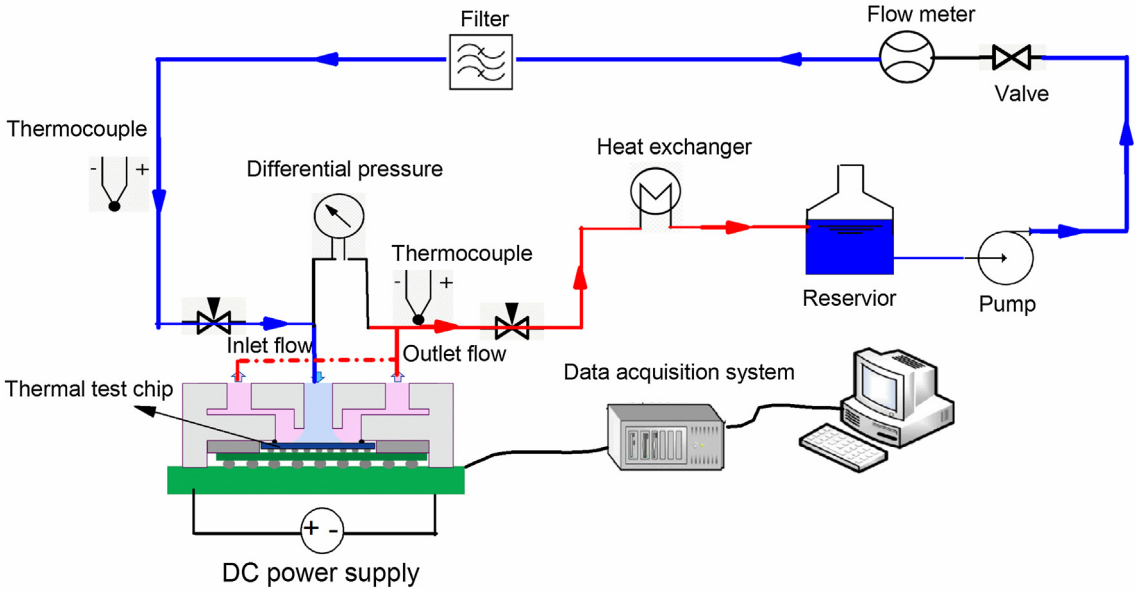

Fig. 6. Schematic of the experimental flow loop.

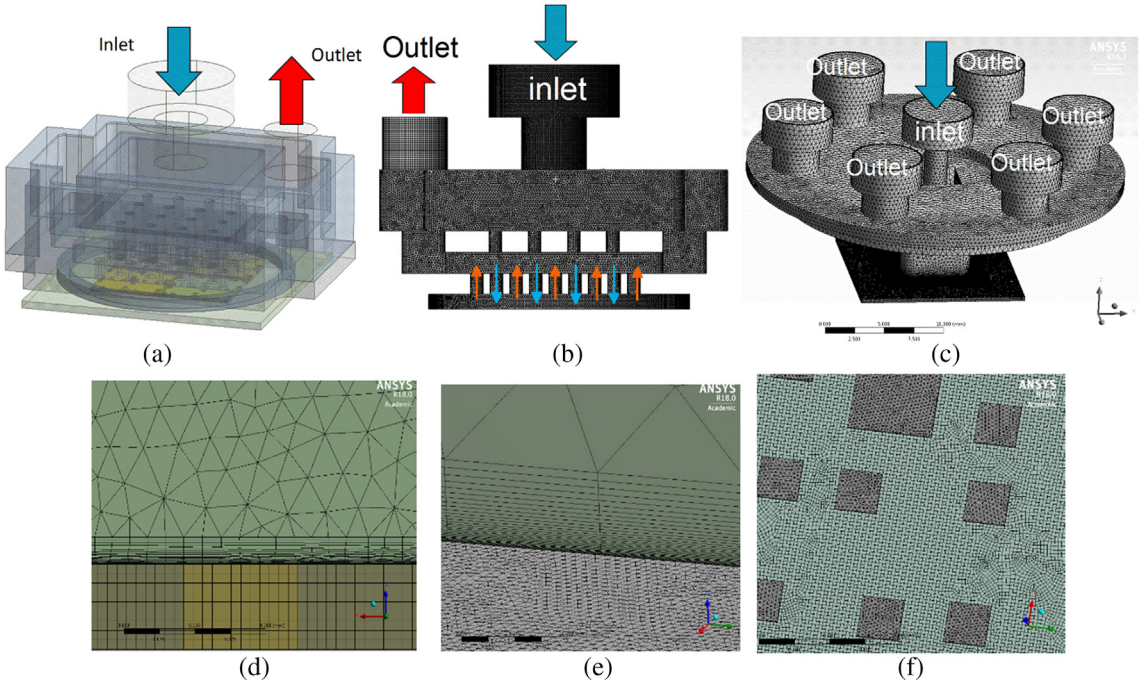

Fig. 7. CFD models: (a) transparent view and (b) meshing of full 4×4 nozzle array models; c) meshing of a single jet cooler with one inlet nozzle and 6 outlet nozzles; (d), (e) and (f) details of the boundary layer and heater cell meshing.

Table 4
Grid convergence index analysis for the model of the single jet cooler.

Temperature	GCI_{12}	Asymptotic range of convergence
Stagnation Temp	0.0019	0.9984
Averaged Temp	0.0043	1.0012

thermal resistance measurements.

In order to accurately estimate the heat transfer coefficient, the heat losses need to be characterized to identify the amount of heat absorbed by the coolant. Since the measurement of the coolant outlet temperature did not result in accurate results an alternative approach was used. The chip temperature profile was first measured for the assembled cooler without any coolant present in the cooler. This case, with an equivalent thermal resistance R_{loss} of 16.8 K/W represents the heat removal from the generated heat through the considered heat losses only. For any liquid cooling measurement with the cooler, the heat losses can now be estimated as follows:

$$Q_{loss} = (T_{chip} - -T_{amb})/R_{loss} \quad (2)$$

Based on the net power (Q_{heater} -Q_{loss}) and the assumed one-dimensional heat conduction across the chip thickness t_c, the average chip surface temperature $\bar{T}_s$ can be estimated as follows:

$$\bar{T}_s = \bar{T}_h - \frac{(Qheater - Qloss) * t_c}{A_{heater} * k_{si}} \quad (3)$$

where $\bar{T}_h$ is defined as the average temperature of the heat source, k_{si} is the thermal conductivity of silicon (k_{si} = 149 W/mK), A_{heater} is defined as the area of the heaters (8 mm × 8 mm × 75%).

The area-averaged heat transfer coefficient $\bar{h}$ is then defined as

$$\bar{h} = \frac{(Qheater - Qloss)}{A_{heater} * \Delta T} \quad (4)$$

$$\Delta T = \bar{T}_s - T_{in} \quad (5)$$

where $\bar{T}_s$ is the average chip surface temperature, T_{in} is the inlet temperature. The temperature difference $\Delta T$is defined as ($\bar{T}_s$-T_{in}) [34]. The Nusselt number $N\bar{u}_d$ and Reynolds number Re_d are both defined based on the inlet nozzle diameter as the characteristic length:

$$Re_d = \frac{\rho d_i \bar{V}_{in}}{\mu}; N\bar{u}_d = \frac{\bar{h} d_i}{k} \quad (6)$$

where $\bar{V}_{in}$ is the average inlet jet velocity, d_i is chosen as the characteristic length, and also k is the thermal conductivity of the fluid.

4. Thermal characterization and model validation

4.1. Quasi-uniform heating

A uniform power dissipation pattern is most suited to characterize the resulting temperature distribution map of a cooling solution since the impact of the thermal spreading in the Si chip is minimal. Fig. 8(a) shows the measured temperature increase distribution map with the single jet cooler for a flow rate of 600 ml/min. The 240 μm resolution of the sensor array allows to accurately capture the temperature profile below the liquid jet: the lowest temperature is observed in the stagnation region while the heat transfer decay along the wall jet region is also clearly visible. The measurement of the full chip temperature distribution allows the evaluation of the maximum, the minimum and the average temperature over the chip area which exhibits a large temperature gradient in this case. The thermal resistance based on the average chip temperature of the single jet cooler is 0.32 K/W for 600 ml/min, for a modeled pressure drop of 0.4 kPa.

The measurement data show an asymmetrical temperature profile, which is caused by the misalignment of the cooler assembly. The same misalignment between the cooler and the test chip center of 0.24 mm has been included in the full cooler level CFD model of the single jet cooler. As shown in Fig. 8(b), the CFD simulation results can accurately predict the stagnation temperature below the jet as well as the temperature increase along the wall jet region for the different flow rates (Re_d = 4286 for 600 ml/min). In Fig. 8(c) the temperature profile from the test chip is compared for the CFD modeling results and the measurement data in the sensors for three different flow rates. The thermal resistance improves by a factor of 2.9 when the flow rate is increased from 200 ml/min to 600 ml/min. It can be seen that the maximum

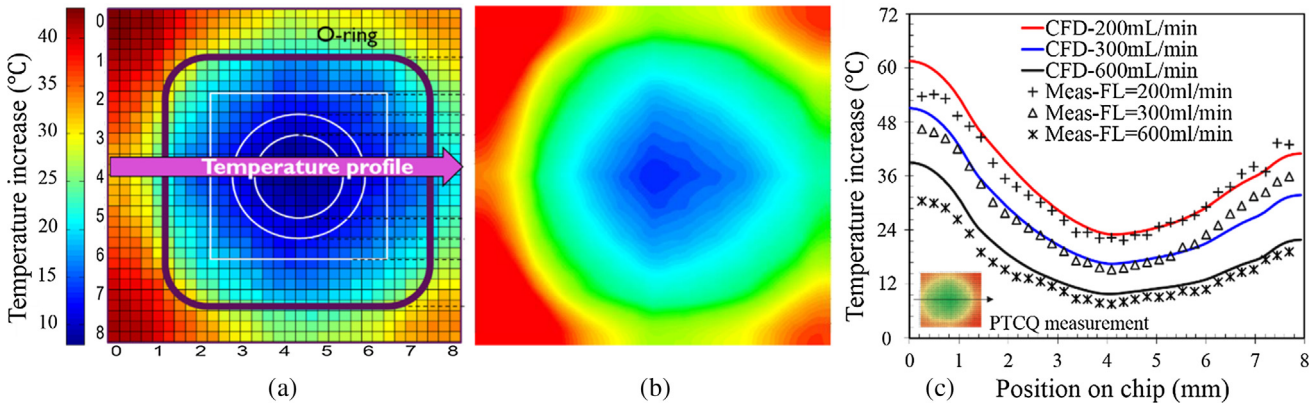

Fig. 8. Single jet model validations (flow rate = 600 ml/min, chip power = 24 W): (a) temperature measurement results; (b) CFD modeling results; (c) comparison of single jet modeling results and experiments data.

errors for the comparison between the single jet modeling results and experimental data are 13.4% (200 ml/min), 8.7% (300 ml/min) and 25.2% (600 ml/min) at the chip edges, while the maximum errors for the stagnation temperature are 3.9% (200 ml/min), 8.8% (300 ml/min) and 10% (600 ml/min). Since the modeling scheme has been successfully validated for the single jet case, it can now be applied to the more complex multi-jet case with distributed returns.

The measured and simulated chip temperature increase maps for the 4×4 jet array cooler are shown in Fig. 9(a) and (b) for a power of 50 W and a flow rate of 600 ml/min. Note that a different scale is used with respect to Fig. 8(a) in order to zoom in on the small variations that are still present. The thermal resistance based on the average chip temperature is 0.25 K/W, for a modeled pressure drop of 15 kPa. Firstly, the temperature asymmetry shown in Fig. 9 is mainly due to the asymmetrical flow since the outlet is located at one side of the cooler. The flow coming from the impingement zone has to be combined together to the outside through outlet tube. Moreover, the O-ring placed under the nozzle plate is fixed as rectangle shape. Secondly, due to the higher heat transfer rate of the cooler compared to the single jet cooler, the location of the heated cells and non-heated cells is visible in the temperature map, revealing a minimum temperature in the central area of the chip where no heater cells are present and lower temperature around the chip periphery. This is caused by the presence of the coolant around the chip in the cavity defined on the chip package. The local minima and maxima of the temperature profile on the chip diagonal can be nicely matched to the location of the inlet and outlet nozzles in Fig. 9(c). It can be seen that the maximum errors for the comparison between the multi-jet modeling results and experimental data are 13.8% for a flow rate of 600 ml/min and 27% for 300 ml/min. The difference between the modeling and measurement results for the average chip temperature is only 4.86% and 4.19% for 300 ml/min and 600 ml/min flow rate respectively. This figure also shows the impact of the flow rate as the thermal resistance reduces by a factor of 1.7 by increasing the flow rate from 300 ml/min to 600 ml/min.

4.2. Hot spots heating

The heat sources in the test chip can also be programmed in a hot spot array pattern. Fig. 10 shows the hot spot cooling results for a 4 × 4 array of hot spots aligned to the 4 × 4 inlet nozzle array: the hot spots consist of 2 × 2 heater cells (480 × 480 μm^2). The chip power is set as 3.3 W for a flow rate 600 ml/min. Fig. 10(a) and (b) respectively show the measured and the modeled chip temperature increase distribution, while the comparison of the temperature profile across four hot spots is shown in Fig. 10(c). The comparison shows that the test chip is capable to accurately capture the local temperature peak of the hot spots, as both the temperature peak values as well as the valleys are clearly resolved. Overall, a good agreement between the modeling and measurement results is found, with a maximum difference of 10% at the peaks. Both the modeling and experimental results exhibit a similar asymmetrical pattern due to the presence of the outlet connector at only one side of the cooler.

5. Results and discussion

5.1. Uniform and quasi-uniform heating

Including a large level of detail on the small heater cells in the CFD

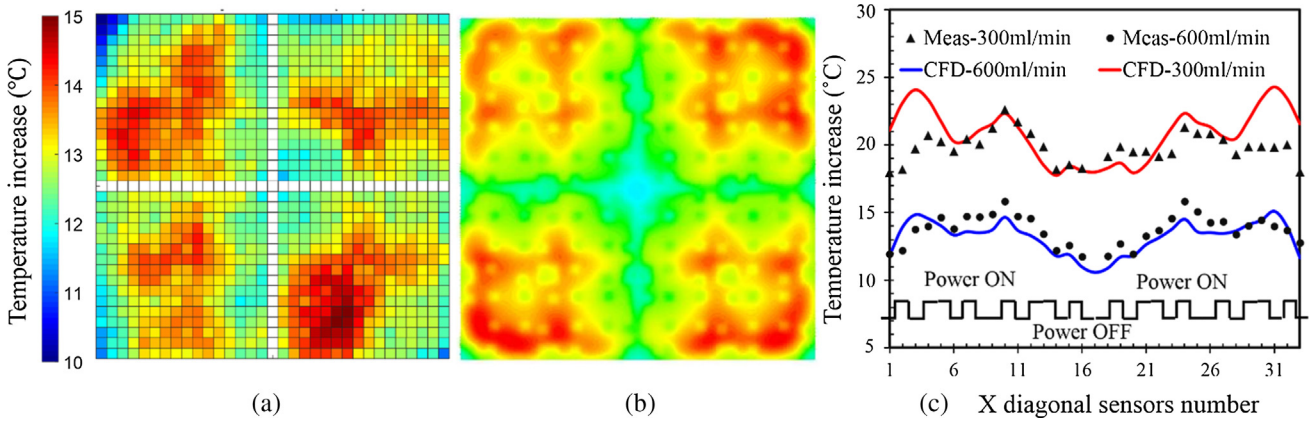

Fig. 9. Modeling and experimental results of 4 × 4 multi-jet cooler (Re_d = 1015 for 600 ml/min) (a) measurement, (b) CFD modeling, (c) temperature increase profile comparison between measurements and CFD modeling of multi-jet cooler (chip power = 50 W).

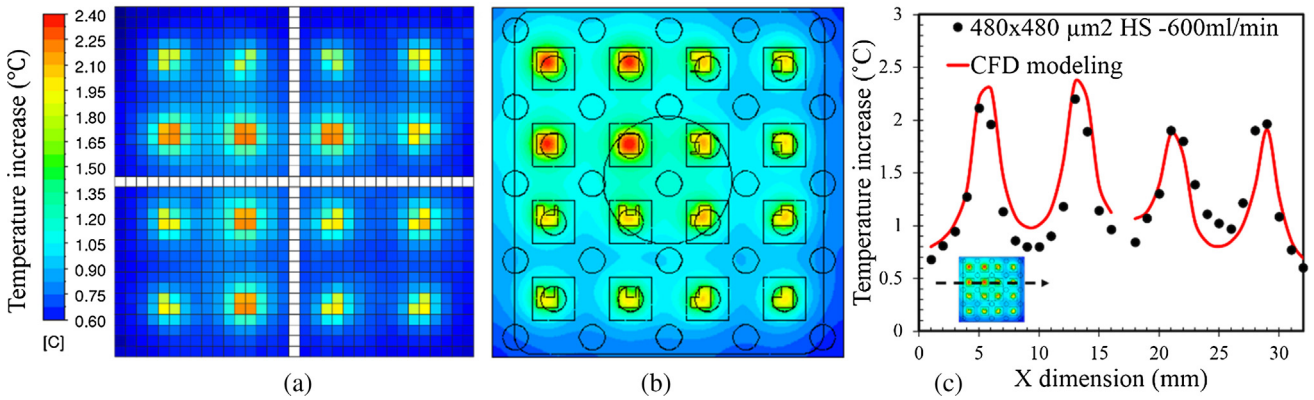

Fig. 10. Experimental and modeling results of 480 × 480 μm^2 hot spots under the chip power Q = 3.3 W (Re_d = 1015 for 600 ml/min): (a) experimental results of local temperature distribution; (b) CFD simulations of local temperature distribution; (c) experiments and modeling comparison under the same flow rate 600 ml/min, and same chip power: Q = 3.3 W.

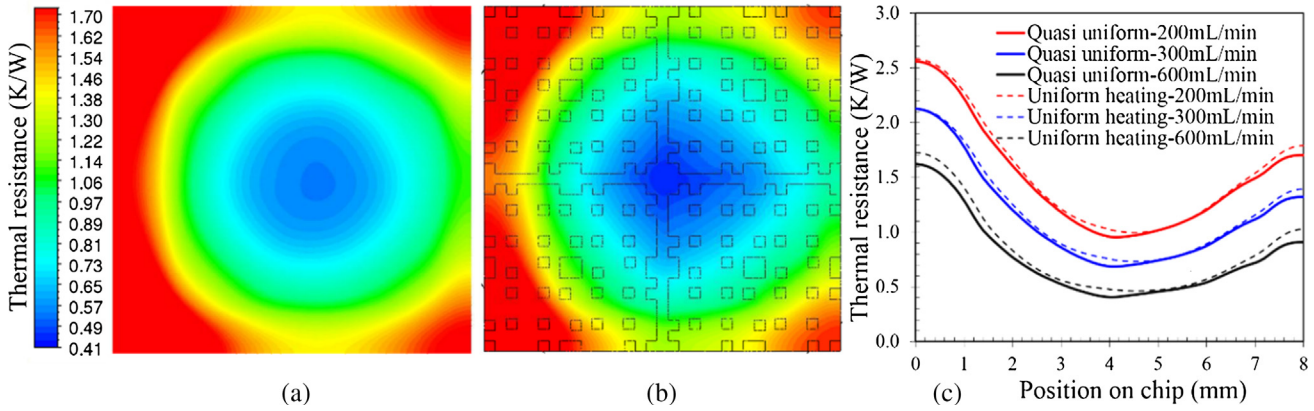

Fig. 11. Comparison of the simulated chip temperature distribution for single jet cooling with different heating configurations: (a) uniform heating modeling results for 600 ml/min; (b) quasi-uniform heating modeling results for 600 ml/min; (c) diagonal profile comparison between uniform heating and quasi-uniform heating (chip power = 24 W).

model will increase the number of elements, and therefore the computation cost. In this section, the accuracy of the CFD model with quasi-uniform heating (75%), including the detailed location of all heater cells or uniform heating (100%) with the same total power, will be compared for different flow rates. In Fig. 11, the comparison of the simulated chip temperature distribution with uniform heating shown in Fig. 11(a) and quasi-uniform heating in Fig. 11(b) is shown for the single jet cooler case. For this moderate cooling condition, the introduction of the heater details in the model does not have a large impact on the temperature distribution. The profiles for the uniform and quasi-uniform heating shown in Fig. 11(c) are very similar with only local differences of 14.6% and 6.7% at the locations where no heaters are present for the flow rates of 600 ml/min and 200 ml/min respectively.

Fig. 12 shows the comparison between the uniform heating case and the quasi-uniform heating case for the 4 × 4 multi-jet cooling. Although the difference for the average temperature is small (10.5% and 1.2% for 300 ml/min and 600 ml/min respectively), the temperature distribution maps look completely different. While in the case of uniform heating shown in Fig. 12(a), the nozzle pattern is clearly visible, the pattern of heated and non-heated cells is visible in the case of quasi-uniform heating shown in Fig. 12(b), due to the high cooling rate of the jet impingement on the surface of the Si chip. The comparison of the temperature profiles along the chip diagonal with the measurement data in Fig. 12(c), reveals that the uniform model is not capable to correctly predict the local temperature distribution. The quasi-uniform model with the complete details on the heater cells shows a much better agreement with the experimental data. This analysis for the single jet cooler and multi-jet cooler clearly shows the need to include sufficient details on the heater structures in the CFD model in order to accurately predict the local temperature distribution in case of high heat removal rates at the chip surface, while for lower heat removal rates a simpler model with uniform heating can be sufficient. Furthermore, the comparison highlights the importance of test structures with a high spatial resolution in order to detect these effects.

5.2. Hot spots cooling modeling

The experimentally validated hot spot model can now be used to evaluate different cooler configurations:

1. Common outlets: in this case there are no local outlets in between the inlet nozzles. The common outlets are located at the edges of the chip shown in Fig. 13(a).
2. Locally distributed outlets in between the inlet nozzles that are aligned to the hot spots shown in Fig. 13(b).
3. Locally distributed outlets in between the inlet nozzles that are intentionally misaligned with the hot spots shown in Fig. 13(c).

Fig. 13(d) shows that the hot spots cooling with locally distributed outlets can achieve a better cooling performance than common outlets. The main advantage of the locally distributed outlets is that the cross flow effects can be reduced that are present in the common outlet flow. The simulation results for the aligned and misaligned hot spots with respect to the nozzle locations show that it is important to align the cooling nozzles with the hot spots, as shown in Fig. 13(d). The

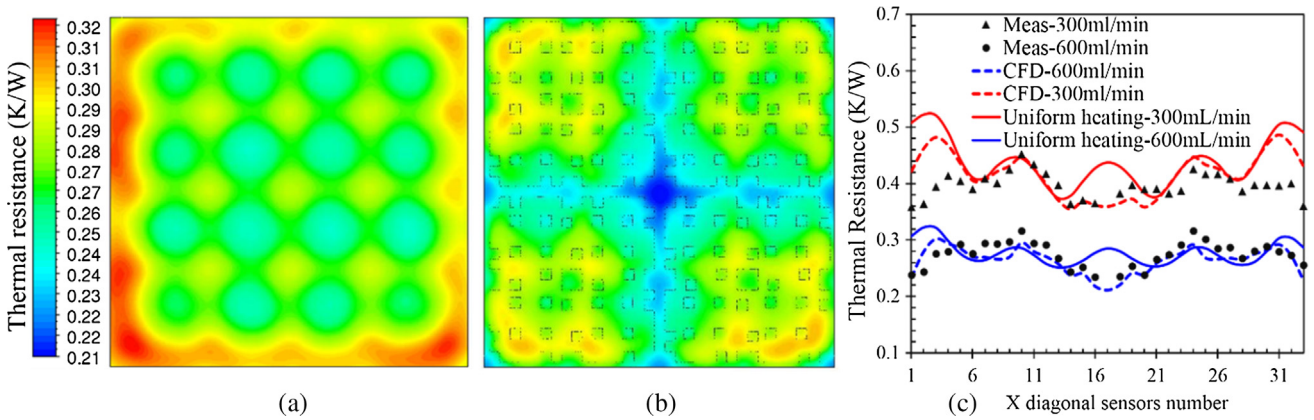

Fig. 12. Comparison of simulated chip temperature distribution for multi-jet cooling with different heating configurations: (a) uniform heating modeling results for 600 ml/min; (b) quasi-uniform heating modeling results for 600 ml/min; (c) profile comparison between uniform heating and quasi-uniform heating (chip power = 50 W).

temperature difference amounts to 10% between aligned and misaligned jet nozzles with the hot spot locations, illustrating the need for a matching design between the nozzle array and the chip floor plan.

5.3. Single jet and multi-jet cooling

As shown in Fig. 14(a), the thermal resistance without liquid cooling is taken as the reference case with regard to the single jet cooling under three different flow rates. The comparison with the single jet cooler on the same chip package in Fig. 14(b), shows that the multi-jet impingement cooler results in a lower thermal resistance and a better temperature uniformity for the same flow rate. The thermal performance of the coolers can also be expressed in terms of the Nusselt number $N\bar{u}_d$ and the Reynolds number Re_d, based on the nozzle diameter as characteristic length, shown in Fig. 15. The following correlations have been extracted for the three different considered coolers:

- 4 × 4 cooler: $N\bar{u}_d = 1.63*Re_d^{0.57}$ (experimental data)
- Single jet: $N\bar{u}_d = 0.54*Re_d^{0.56}$ (experimental data)
- 4 × 4 cooler (Common outlets): $N\bar{u}_d = 1.34*Re_d^{0.59}$ (modeling data)

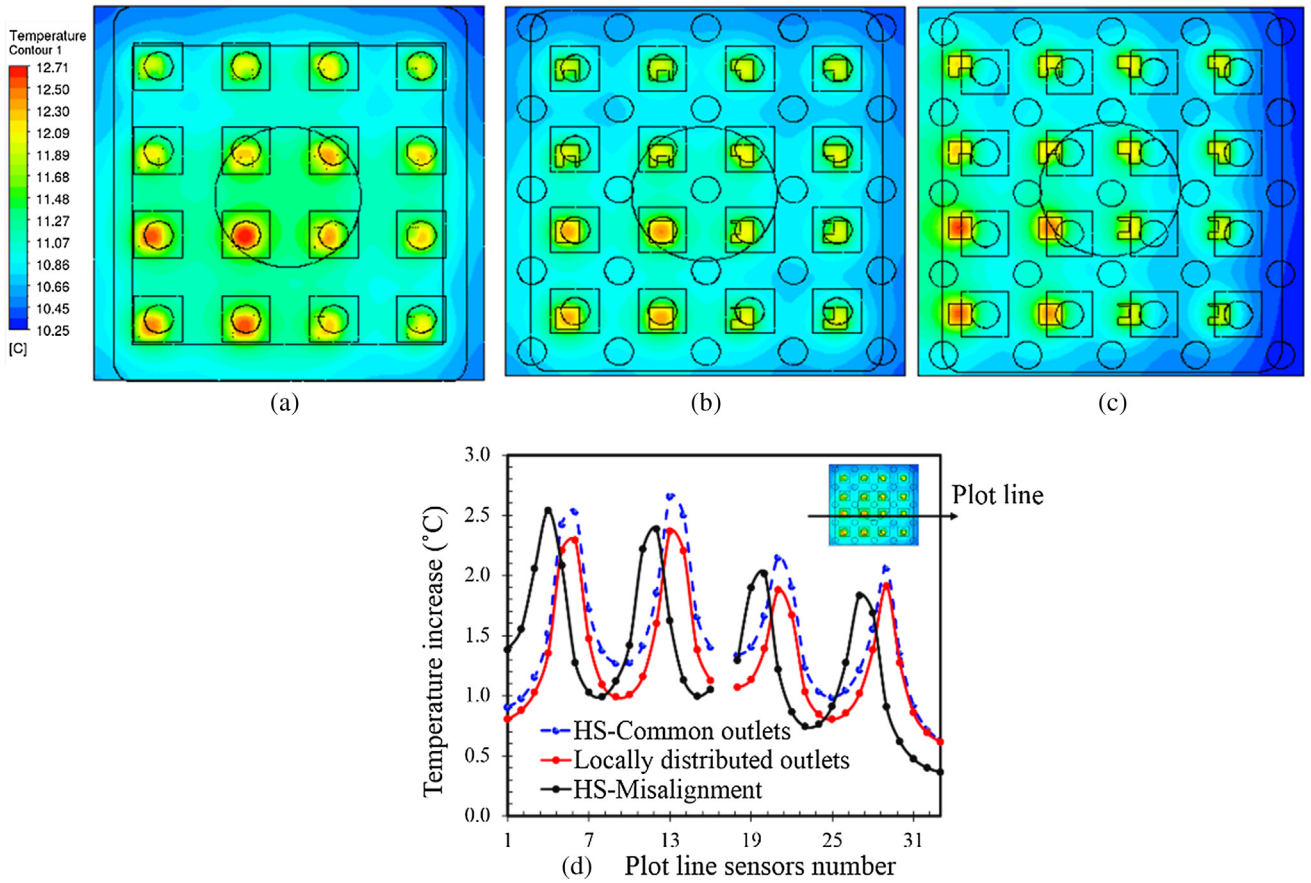

Fig. 13. Hot spots cooling modeling for flow rate 600 ml/min: (a) hot spots cooling with common outlets; (b) hot spots cooling with locally distributed outlets; (c) hot spots cooling with nozzle misalignment; (d) temperature profile comparison with different configurations.

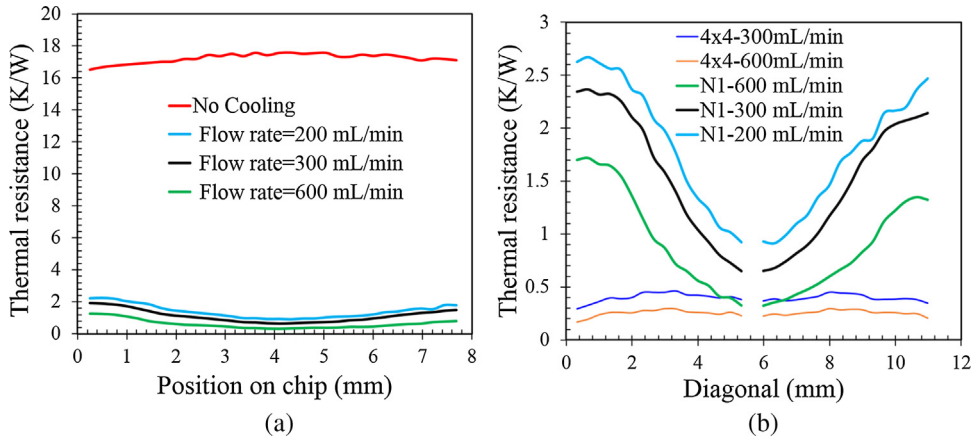

Fig. 14. Normalized comparison of the measured temperature profiles for the cases of (a) single jet cooler with respect to the reference measurement without cooling; (b) comparison between the singe jet cooling and multi-jet 4 × 4 array cooling.

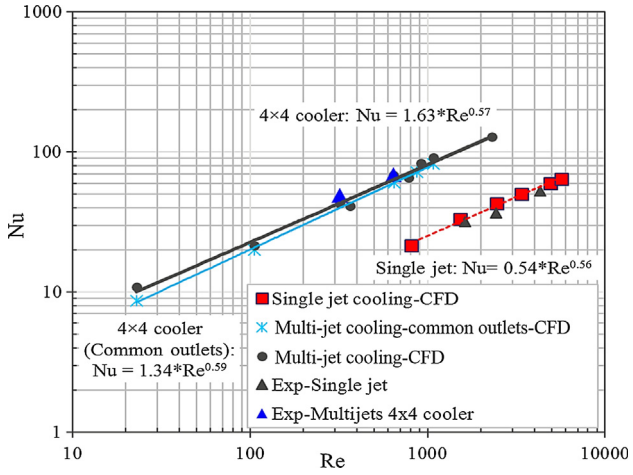

Fig. 15. Correlations between Nusselt number and Reynolds number for single jet and multi-jet configurations.

An extensive overview of heat transfer correlations for jet impingement cooling is available in [1] in the form of:

$$Nu = c.\ Re^{m} \quad (7)$$

For all these correlations, the exponent m is within the range of 0.48–0.8. The obtained exponents of the correlations for the coolers studied in this work are within this range.

6. Conclusions

In this work, a 8 × 8 mm^2 thermal test chip with programmable heat dissipation maps and an array of 32 × 32 diodes as temperature sensors is presented. This test chip allows to apply custom power dissipation patterns such as quasi-uniform heating or hot spot patterns using the 832 individually addressable heaters in order to evaluate different applications. The chip temperature distribution can be measured with a spatial resolution of 240 μm, allowing the accurate capturing of local temperature effects on the chip. In this way, the test chip combines the advantage of optical temperature measurement techniques (providing a full chip temperature distribution map) with the advantages of using integrated thermal test vehicles (testing of the cooling solution on integrated chip packages in realistic environments).

The thermal test chip has been applied for the thermal analysis and the CFD model validations for two liquid jet impingement coolers: 1) a single jet cooler with a 2 mm diameter nozzle, and 2) a multi-jet cooler with a 4 × 4 array of 500 μm inlet nozzles and distributed outlet nozzles. The detailed temperature map measurements show that the multi-jet impingement cooler achieves a lower thermal resistance and a better temperature uniformity for the same flow rate compared to the single jet cooler. For the 4 × 4 array cooler, a very low thermal resistance of 0.25 K/W is obtained for a flow rate of 600 ml/min with a required pump power of 0.4 W. Furthermore, the comparison of the detailed temperature map measurements with the CFD modeling results, indicates the need to include sufficient details on the heater structures in the CFD model in order to accurately predict the local temperature distribution in case of high heat removal rates at the chip surface for the multi-jet cooler, while for lower heat removal rates with the single jet cooler, a simpler model with uniform heating can be sufficient.

The validated CFD model of the multi-jet coolers has been applied to evaluate different nozzle configurations for the hot spots test case. The analysis shows that the coolers with distributed outlets achieve better cooling performance than coolers with common outlets since the cross flow effects can be reduced. Moreover, it is shown that the misalignment of the nozzles with the hot spot locations results in a temperature increase of 10%, indicating the need for a matching design between the nozzle array and the chip floor plan. Finally, the measurement results on the single jet and multi-jet cooler have been used to derive the Nusselt correlations after correction for the heat losses in the cooler assembly. The obtained correlations are $\bar{Nu}_d = 1.63{*}Re_d^{0.57}$ and $\bar{Nu}_d = 0.54{*}Re_d^{0.56}$ for the multi-jet and single cooler respectively.

Appendix A. Supplementary material

Supplementary data to this article can be found online at https://doi.org/10.1016/j.applthermaleng.2019.02.075.

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