Experimental and Numerical Study of 3-D Printed Direct Jet Impingement Cooling for High-Power, Large Die Size Applications

Tiwei Wei, *Member, IEEE*, Herman Oprins, *Member, IEEE*, Vladimir Cherman, *Member, IEEE*, Zhi Yang, Kathryn C. Rivera, Geert Van der Plas, *Member, IEEE*, Bartlomiej J. Pawlak, Luke England, Eric Beyne, *Senior Member, IEEE*, and Martine Baelmans

***Abstract*— In this article, we design, demonstrate, and characterize a 3-D printed package-level polymer jet impingement cooling solution on a 23 × 23 mm^2 thermal test chip. The experimental hardware results for a nozzle pitch of 2 mm show that, with 1-kW power dissipation, at a coolant (deionized (DI) water) flow rate of 3 liters per minute (LPM), the measured average chip temperature increase is ∼65 °C with a cooler pressure drop of 0.15 bar between the inlet and outlet connections. It is also shown that bare die cooling without lid [and thermal interface material (TIM)] shows better cooling performance than the lidded package. Second, an advanced 3-D printed manifold with an additional flow redistribution structure is demonstrated. The experimental results show that the improved design achieves a better chip temperature uniformity compared to the reference design, showing a reduction of the chip temperature gradient with a factor of 4 and 2.3 for a flow rate of 0.5 and 3 LPM, respectively, while no significant impact on the cooler pressure drop was measured. The numerical modeling studies predict an additional 15.4% thermal performance improvement, by reducing the nozzle pitch from 2 to 1 mm, for a flow rate of 3 LPM.**

***Index Terms*— 3-D printing, flow uniformity, impingement cooling, large die.**

I. Introduction

ACTIVE liquid cooling is regarded as an efficient cooling technique that can cope with the increasing power density values of electronic devices [1]. Regarding liquid forced convection cooling, the current advanced solutions include three major types [2], as shown in Fig. 1. The first type shown in Fig. 1(a) is using a liquid cold plate heat sink attached to the lid, where there will be two thermal interface material (TIM) layers in between the cooling solution and the chip. With a directly attached liquid cold plate on the die [see Fig. 1(b)], there is only one TIM layer between the liquid cold plate and the chip backside [2]. However, the main drawbacks of these two liquid cooling solutions are: 1) the presence of the TIM, which represents a significant thermal resistance contribution [2], [3]; 2) the temperature gradient along the chip surface, since the coolant can be heated up along cooling channel; and 3) the pressure drop inside the channel is scaling with the channel length, resulting in a higher pressure drop for large cooling channels. Even though significant progress has been made on the increase of the TIM thermal conductivity, the total TIM thermal resistance, including the thermal contact resistance between the TIM and the die and between the TIM and the cooler, is large [3]. As a third and fourth option, the bare die backside cooling by embedded microchannel cooling and impingement jet cooling shown in Fig. 1(c) can eliminate the TIM layers as the coolant directly contacts the bare chip or component. The schematic of the bare die impingement jet cooling is shown in Fig. 2, illustrating the inlets and outlets locations inside the cooler. The experimental data from the literature show that bare die jet impingement cooling can increase the heat transfer coefficient up to 8.7×10^4 W/(K·m^2) [4]. However, the drawback of these Si-based microjet impingement coolers is the high pressure drop for the small diameter nozzles and the high fabrication cost.

In our previous studies [5]–[7], we have shown that additive manufacturing can be applied to create polymer-based impingement coolers with sub-mm nozzles that are more energy efficient than silicon-based coolers. The demonstrators are summarized in Fig. 3. The multijet coolers shown in Fig. 3(b) and (c) can achieve heat transfer coefficients up to 6.25×10^4 W/(m^2·K) with a pump power as low as 0.3 W [5], [6]. Moreover, 3-D printing of complex internal structures, such as manifolds and channels, enables the reduction of the pressure drop while keeping the same cooling performance [7].

With the increasing demand for the functionality and higher computation performance for high-performance chips, the die

Manuscript received August 17, 2020; revised November 13, 2020; accepted November 21, 2020. Date of publication December 16, 2020; date of current version March 19, 2021. This work was supported in part by the imec Industrial Affiliation Program on 3-D System Integration and in part by the imec partners and the imec Reliability, Electrical Testing, Modeling and 3-D Technology teams. Recommended for publication by Associate Editor S. H. Bhavnani upon evaluation of reviewers' comments. *(Corresponding author: Tiwei Wei.)*

Tiwei Wei is with the Department of Mechanical Engineering, KU Leuven, 3001 Leuven, Belgium, and also with IMEC, 3001 Leuven, Belgium (e-mail: tiwei32@stanford.edu).

Herman Oprins, Vladimir Cherman, Geert Van der Plas, and Eric Beyne are with IMEC, 3001 Leuven, Belgium.

Zhi Yang, Kathryn C. Rivera, and Luke England are with GlobalFoundries, Malta, NY 12020 USA.

Bartlomiej J. Pawlak is with GlobalFoundries, Malta, NY 12020 USA, and also with GlobalFoundries, IMEC, 3001 Leuven, Belgium.

Martine Baelmans is with the Department of Mechanical Engineering, KU Leuven, 3001 Leuven, Belgium (e-mail: martine.baelmans@kuleuven.be).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCPMT.2020.3045113.

Digital Object Identifier 10.1109/TCPMT.2020.3045113

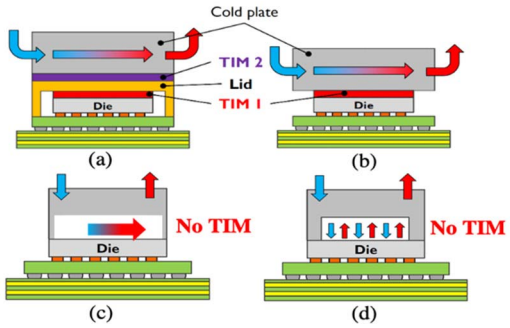

Fig. 1. Schematic of the advanced liquid cooling solutions. (a) Liquid cold plate heat sink on the lid. (b) Directly attached liquid cold plate. (c) Bare die embedded microchannel cooling. (d) Bare die backside cooling by impingement [2].

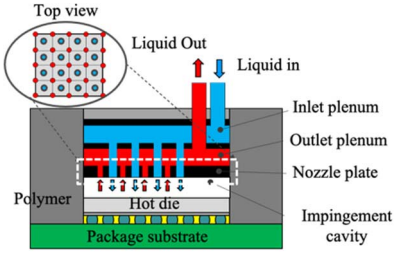

Fig. 2. Schematic of the impingement jet cooling with cross-sectional view and top views, illustrating the i intermixed patterns of the inlets and outlets [3].

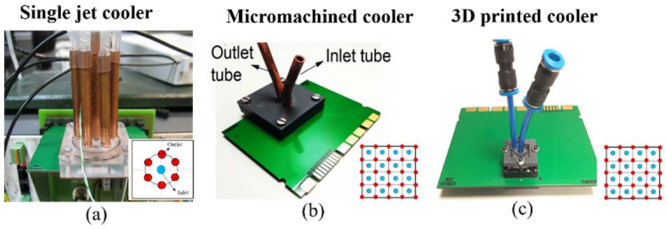

Fig. 3. Schematics of the polymer impingement coolers on the 8 × 8 mm^2 test chip. (a) Single jet cooler with mechanical micromachining process [6]. (b) 4 × 4 multijet cooler with micromachining technique [5]. (c) 3-D printed multijet cooler with 4 × 4 arrays [7].

size has significantly grown over the years [8]–[15]. The die size has increased from 12 mm^2 in 1971 to 688 mm^2 in 2019 for Intel microprocessors and from 270 mm^2 in 1998 to 696 mm^2 in 2019 for International Business Machines Corporation (IBM) microprocessors. For traditional microchannel cooling with coolant flow parallel to the chip surface, it is very challenging to maintain a small temperature gradient over the chip area for large die size applications. An additional concern for large die applications is the warpage of the chip and the package during the cooler assembly. While jet impingement coolers outperform liquid cooling solutions with channels parallel to the chip surface in terms of chip temperature distribution, obtaining good flow uniformity over all the impinging jets becomes more challenging as the die area increases. Innovative channel designs have been introduced to improve the flow distribution, such as bifurcation H-designs with equal distance from the feeding channel to each nozzle [16]–[18] or hybrid microjet heat sinks formed by a pair of fractal channel manifolds, used as liquid inlet and outlet conduits. The experiments and numerical modeling results show that the flow uniformity can be improved at the expense of an increased pressure drop [19], [20]. In [21], an additively manufactured metal porous module with a tree-like microchannel was introduced to uniformly distribute the liquid coolant that was from the central coolant inlet to the whole heated surface of the die. However, this branched design requires an extra level layer that will increase the cooler size and results in an increased pressured drop.

High pressure drop will increase the system pump power that consumes much more electricity and costs. It also has the potential to cause stress on the device, resulting in mechanical reliability problems. The 3-D printing offers the flexibility of designing internal structures to improve the flow uniformity of the cooler with lower pressure drop and shows the potential to overcome the cooler design challenges for large die applications. In our previous study, it has been proved that the flow uniformity can be improved by carefully designing the inlet manifold structures for multichip 2.5-D interposer packages [3]. However, the previous demonstrations are all based on the small footprint of an 8 × 8 mm^2 thermal test chip. This article will demonstrate the application of the multijet cooling concept for a realistic large die size and high chip power values. Specifically, this article will present the design, fabrication, experimental characterization, and modeling study of a package-level multijet cooler for large die sizes, fabricated using 3-D printing. Two versions of the large die cooler design are discussed in this article. The first cooler version, referred to as the reference cooler, is the scaled-up design of the 8 ×8 mm^2 chip cooler [5]–[7] to a much larger die size. The thermal and hydraulic performance of the reference large die coolers with and without lid is characterized and analyzed in Section IV-A. The second version of the cooler, referred to as the improved cooler design, has an additional distribution layer to improve the coolant flow uniformity. In Section IV-B, the thermohydraulic performance of the improved large die cooler is characterized and compared with the reference cooler. In Section IV-C, high-power measurement with 1 kW is investigated. In Section VI, the thermal and hydraulic impact of the reduction of the nozzle pitch is explored.

II. Large Die Cooler Design and Demonstration

A. Large Die Size Thermal Test Vehicle

In order to evaluate the package-level large die cooler performance, a passive thermal test chip [22] with a footprint of 23 × 23 mm^2 is used. The test chip contains 16 metal meander resistor heaters, with a resistance of 8 Ω, and 25 temperature sensor resistors. The calibrated temperature coefficient of resistance (TCR) of the sensors at a reference temperature T_0 of 25 °C is 3553 ± 2 ppm/°C in the temperature range from 10 °C to 75 °C. The test chip is flip-chip mounted on a package laminate substrate of 55 × 55 mm^2. For the lidded packages, a 1-mm-thick Cu lid is glued on the top of the silicon die. Fig. 4(a) shows the image of a lidded package of the thermal test die. The heater zones and the locations of the temperature sensors are shown in Fig. 4(b) and (c), respectively.

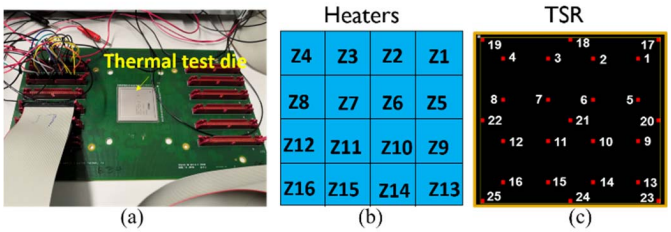

Fig. 4. 23 mm × 23 mm thermal test chip with 16 heater zones and 25 temperature sensors. (a) Lidded package with 55 × 55 mm^2 package substrate, assembled to the test board. (b) Heater zones layout. (c) Temperature sensors layout [22].

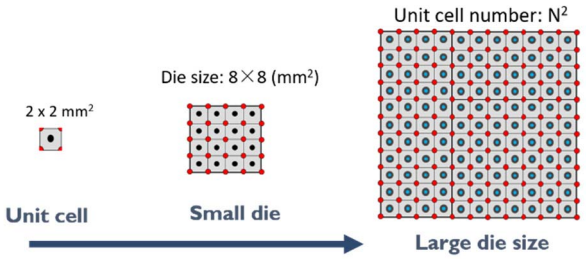

Fig. 5. Scaling unit cell to large die size cooler design. (a) Unit cell size [23]. (b) Small die size with 8 × 8 mm^2 [5]–[7]. (c) Large die size with 23 × 23 mm^2.

B. 3-D Printed Cooler Design and Challenges

For the cooler design structure, there are four main regions: inlet plenum, outlet plenum, nozzle plate, and impingement region. The inlet plenum is used as the divider for the incoming liquid, where the liquid is fed into different inlet nozzles. The outlet plenum is used as the collector, for the collection of all the liquid from the outlet channels. The nozzle plate contains the $N \times N$ nozzles arrays shown in Fig. 5. The impingement jet region is the space between the nozzle plate and the chip cooling surface.

For the design of the inlet and outlet nozzle array in the nozzle plate, we previously introduced the unit cell modeling approach to understand the thermal and hydraulic behavior inside one unit cell, consisting of one central inlet nozzle and four outlet nozzles. With the assumption of uniform flow rate for each individual inlet nozzle and consequently identical thermal and hydraulic performance of each unit cell, the unit cell approach can be used to predict the average chip temperature for arbitrary chip sizes, by scaling the number of unit cells and the flow rate per unit cell. The previously demonstrated microjet coolers with a 4 × 4 inlet nozzle array based on the 8 × 8 mm^2 thermal test die size showed a good agreement with the unit cell model with a unit size of 2 × 2 mm^2 [5]–[7]. For this study with the 23 × 23 mm^2 test vehicle, the nozzle array is a scale to an 11 × 11 inlet nozzle array maintaining the same nozzle diameter and pitch values. The bottom view of the jet nozzle plate shown in Fig. 5 thus contains an 11 × 11 inlet array and a 12 × 12 array of outlets distributed in between the inlets, with a nozzle pitch of 2 mm and a nozzle diameter of 600 μm. However, the challenges for large die cooler design are the flow uniformity and chip temperature uniformity as the distance in the plenum increases, which can generate potential warpage across the large die.

Two large die cooler configurations matching the dimensions of the chip package have been designed. The reference cooler design, design 1 [Fig. 6(a)], is the scaled version of the 4 × 4 nozzle array cooler [7] with the same unit cell, obtained by simply scaling the nozzle plate and inlet and outlet plenums according to the chip size. In the reference design, the nozzle plate is located directly below the central coolant entrance connection. Design 2 [Fig. 6(b)] is an improved cooler design with an additional flow distribution layer above the nozzle plate to improve the flow uniformity over the inlet nozzles and, consequently, the chip temperature uniformity.

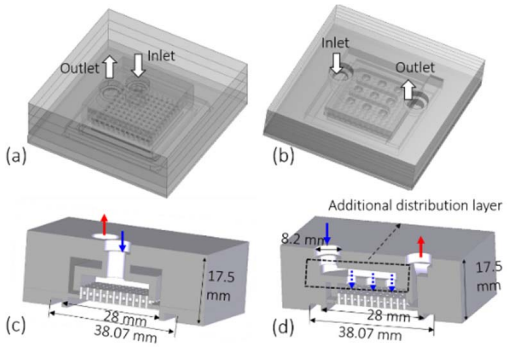

Fig. 6. CAD structure for the large die cooler: an overview of (a) design 1 and (b) design 2. (c) and (d) Cross-sectional view of two microfluidic cooler configurations. Design 1 with nozzle array below coolant entrance connection and Design 2 with additional distribution layer to improve flow uniformity over chip surface.

As shown in Fig. 6(d), this additional distribution layer is implemented as a 3 × 3 array of vertical feeding tubes, which are distributed on top of the 11 × 11 microjet nozzle arrays. For both cooler designs, the cavity height, defined as the nozzle-to-chip surface distance, is 600 μm and the total cooler size is 55 × 55 × 17.5 mm^3. In the cooler assembly, O-rings are used for the sealing between the cooler and the package substrate. A dedicated groove is foreseen in the cooler design for these rings. An additional advantage of the O-rings is that they add some buffer to compensate for the warpage of the large die assembly.

Jet impingement geometries are usually described and characterized by normalizing with respect to the nozzle diameter. Therefore, the dimensionless parameters are also discussed in this paragraph. The baseline array is described as having a nozzle height of 600 μm, a diameter of 0.6 mm, and a pitch of 2 mm. This would result in a dimensionless height of H/D = 1 and a dimensionless pitch of P/D = 3.33.

C. Demonstration of 3-D Printed Large Die Coolers

The large die coolers are 3-D printed using high-resolution Stereolithography (SLA), using the water-resistant material Sonos WaterShed XC 11122 [7]. Fig. 7 shows the side view of the two versions of the transparent coolers, revealing the successfully fabricated internal structures of the two cooler designs, which could not be fabricated with conventional fabrication techniques. The measured average nozzle diameter

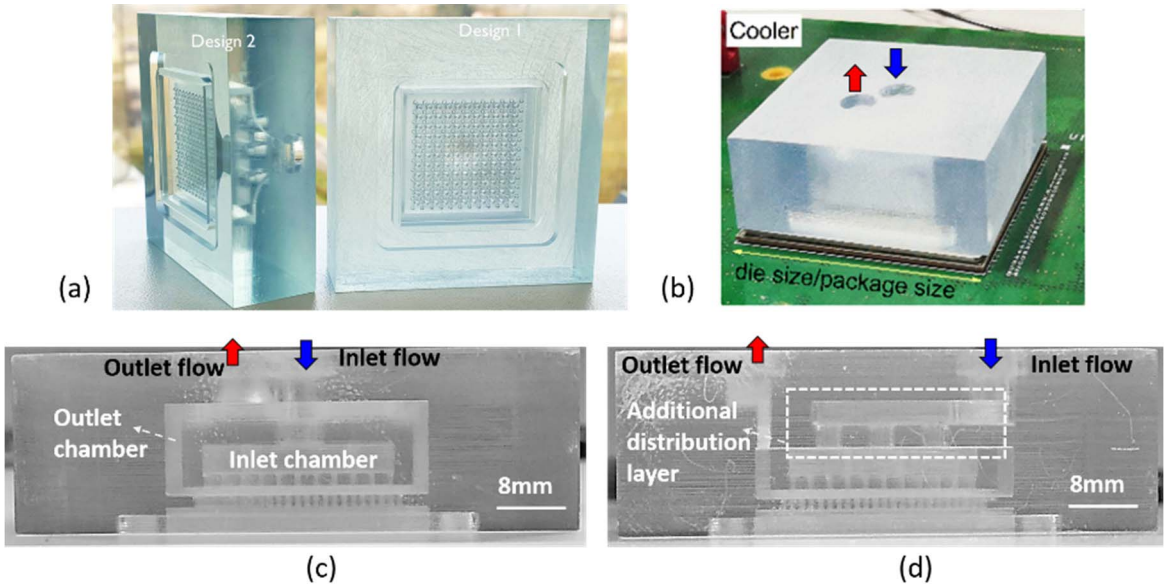

Fig. 7. 3-D printed cooler demonstrations. (a) Images of the demonstrated coolers with designs 1 and 2. (b) Cooler size is matched with large die/package size. (c) and (d) Side view of the transparent fabricated microfluidic heatsinks with internal liquid delivery microchannels.

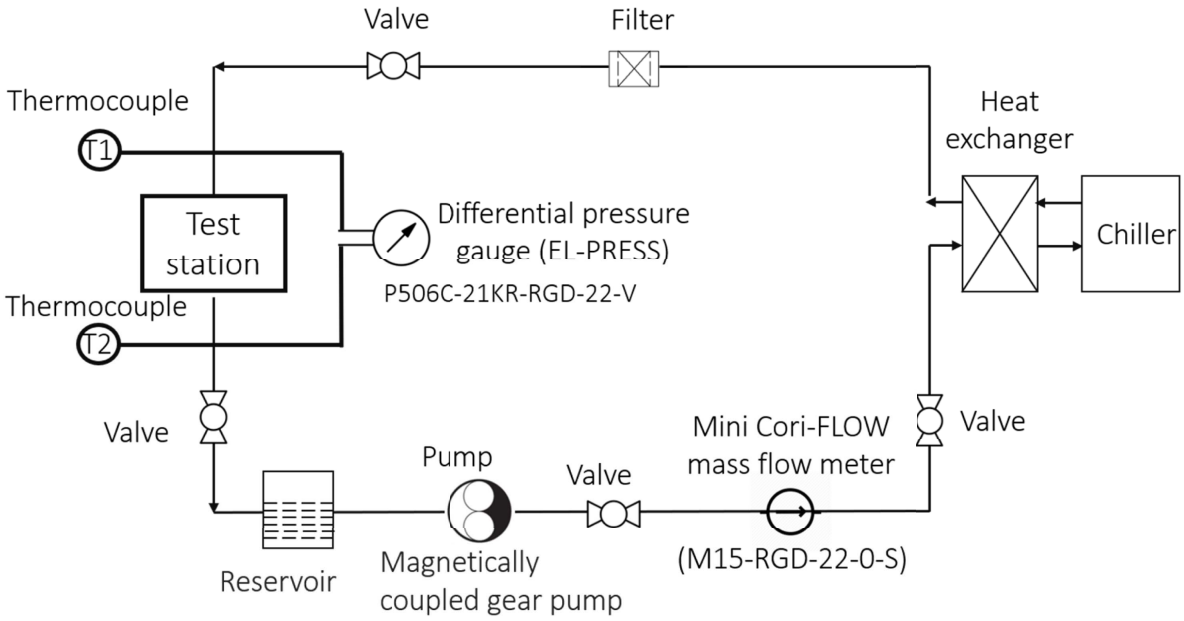

Fig. 8. Configuration of a closed-loop flow system for the experiments. Key components of the flow loop system are pump, flowmeter, pressure transducer, heat exchanger, and chiller.

is 630 μm, which deviates only 5% from the nominal design value of 600 μm. This demonstrates that additive manufacturing can be used for the fabrication of complex large die cooler geometries with microscale features.

III. Experimental Method

A. Large Die Cooler Setup

The assembled coolers are connected to the test board, for providing the electrical power for the heater and measuring the sensor resistance. After that, the assembled cooler will be inserted inside the closed flow loop for which the key components are shown in Fig. 8. As shown in Fig. 9(a), the heat control regions are located in the left part of the test board, whereas the temperature sensor measurement connections are located in the right part. The schematic drawing of the electrical control for the 16 heaters in the large die is shown in Fig. 9(b). All the heaters are connected to a single power supply, with four parallel chains of four heaters in series to dissipate uniform power. Off-chip resistors are designed to measure the current in each branch.

Since the heater resistance is temperature dependent, the value of the resistance and power depends on the applied

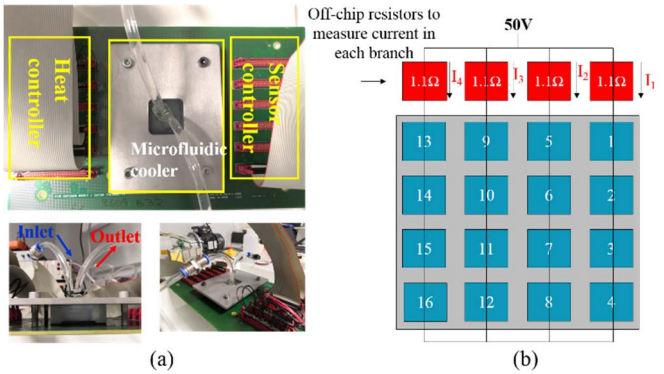

Fig. 9. Measurements setup. (a) Details of the fluidic and electrical connections to the test vehicle in the flow loop. (b) Schematic of the electrical control for the 16 heaters in the large die.

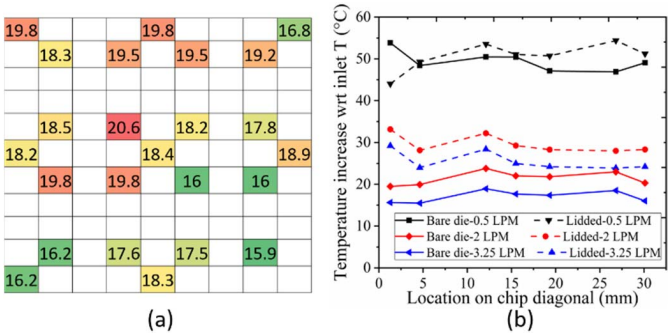

Fig. 10. Temperature measurement on the test chip for a total applied voltage of 50 V using the reference large die cooler with design 1. (a) Temperature distribution map for a constant flow rate of 3 LPM. (b) Temperature profile along the large die diagonal with a total applied voltage of 50 V.

voltage on the heater and the coolant flow rate. For different flow rates and heater voltage values, the current is measured in each of the four branches, and the voltage drop is measured for all 16 heaters. This allows the calculation of the resistance and the power dissipation of each heater. The total heater power can be calculated by adding the 16 resistor values, resulting in 266.8 W for a total applied voltage of 50 V, at a flow rate of 1 L/min. Table I lists the measured total heater power at 50-V heater voltage for different flow rate values. This is due to the heater resistance change with the heater temperature, influenced by the flow rate.

B. Flow Loop System

The configuration of the closed-loop flow system for the experiments is shown in Fig. 8. The key components of the flow loop system are the pump, the mass flowmeter, the differential pressure transducer, the heat exchanger, and the chiller. The magnetically coupled gear pump can work with a maximum flow rate of 3 kg/min and a maximum pressure of 11.5 bar. A mini Cori-FLOW mass flowmeter (M15-RGD-22–0-S) with a range of 0.1–3 kg/min and an accuracy of ±0.2% is used to control the flow rate. A differential pressure gauge (EL-PRESS) with ID of P506C-21KR-RGD-22-V is used to measure the pressure drop between the inlet and outlet of the cooler, with an accuracy of ±0.5%.

TABLE I

HEATER POWER AT 50-V VOLTAGE FOR THE LIDDED PACKAGE AND LIDLESS PACKAGE FOR DIFFERENT FLOW RATES

Flow rate (LPM)	Lidded package Power (W)	Lidless package Power (W)
0.5	252.04	248.39
1	261.50	266.81
1.5	265.67	270.71
2	267.76	273.29
2.5	268.97	274.85
3	269.75	275.37
3.25	269.94	275.73

TABLE II

LIST OF EXPERIMENTAL TOOLS IN THE TEST SYSTEM AND THEIR ACCURACY INFORMATION

Experimental tools	Parameters	Accuracy
Thermocouple (K-type)	Tin	± 5%
Mini Cori-FLOW mass flow meter	Q_{mass}	± 0.2%of rate (Liquid)
Differential pressure gauge (EL-PRESS)	Δp_{-total}	± 0.5% (0.2 -5 bar)
Temperature-sensitive resistors	TSR	3553 ± 2 ppm/°C

The mesh size of the particle filter is 25 μm. The inlet and outlet temperature are measured by the thermocouples with an accuracy of 2.2 °C. The heat exchanger is used to control the inlet temperature as 10 °C.

C. Data Reduction and Uncertainty Study

For the uncertainty analysis of the reported quantities, the uncertainty of all the measurement devices has been considered, and the theory of measurement error propagation has been used. The overall thermal performance of the cooler is expressed in terms of the thermal resistance defined as follows:

$$R_{\text{th}} = \frac{\Delta T_{\text{avg}}}{Q_{\text{heater}} - Q_{\text{loss}}} \tag{1}$$

where ΔT_{avg} is defined as the chip temperature increase and Q_{heater} is the heat generated in the heater cells based on the measured electrical current and heater voltage. This thermal performance estimation of the assembled cooling solution also includes the heat losses through the cooler material into the ambient and the heat losses through the bottom side of the assembled test board.

In the second step, the 25 temperature-sensitive resistors (TSR) are calibrated as a function of temperature. The range of the calibrated temperature is from 10 °C to 70 °C. The calibrated TCR is 3553 ± 2 ppm/°C. Therefore, the temperature increase of the sensor ΔT with respect to the reference temperature T_0 can be determined by the following equation:

$$\Delta T = \frac{R - R_0}{R_0 \cdot \text{TCR}} \tag{2}$$

where R_0 is the resistance at the reference temperature T_0.

Based on the uncertainty analysis of the experimental results shown in Table II, the calculated uncertainty for the chip average temperature increase is 1.5%.

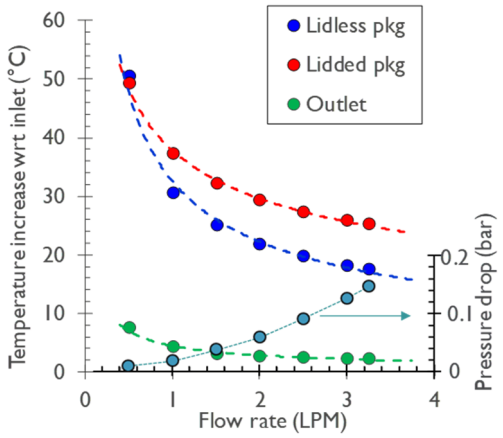

Fig. 11. Temperature and pressure drop measurements at different flow rates (applied voltage 50 V at 3 LPM: 270-W lidded package and 276-W bare die package).

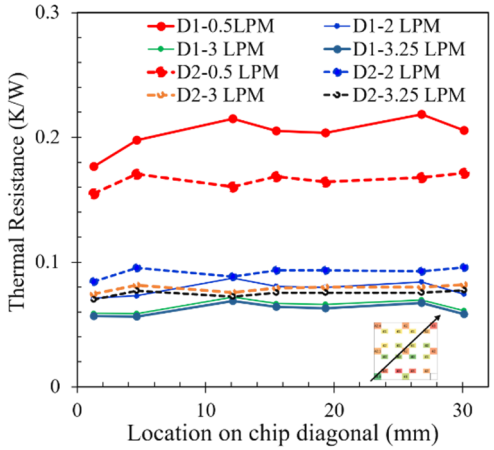

Fig. 12. Temperature profile comparison between designs 1 and 2 from bottom left to top right along the chip diagonal position.

IV. Experimental Characterization

A. Experimental Characterization: Design 1

By using the 24 temperature sensors (1 sensor failed), the temperature distribution across the large die can be captured, as shown in Fig. 10(a) for a chip power of 269 W and a coolant flow rate of 3 liters per minute (LPM). The reported temperature increase is defined as the chip temperature increase with respect to the coolant inlet temperature. The average chip temperature increase is 17.5 °C, which corresponds to a thermal resistance of 0.07 K/W, and the temperature difference between the maximum and minimum temperatures is 4.7 °C.

In Fig. 10(b), the measured chip temperature profiles along the chip diagonal for three different flow rates for a total applied voltage of 50 V are presented. Fig. 10(b) also shows the comparison between the lidded package cooling (dashed line) and bare die cooling (solid line). The difference between the lidded package cooling and the bare die cooling is caused by the additional thermal resistance of the lid and TIM and the additional lateral thermal spreading in the lid.

Fig. 11 summarizes the thermal performance comparison between lidded package cooling and bare die cooling for a heater voltage of 50 V (at 3 LPM: 270-W lidded package and 276-W bare die package). It shows that the lidded package has a slightly better thermal performance at low flow rates, but the bare die cooling significantly outperforms the cooling on the lid at higher flow rate values; for a coolant flow rate of 3 LPM, the temperature increase of the bare die package is 44% lower and the chip temperature gradient is 16% smaller. At these cooling conditions, the average chip temperature increase is as low as 17.5 °C, the coolant temperature increase is 1.5 °C, and the measured pressure drop over the cooler is 0.15 bar.

B. Experimental Characterization: Design 2

This section will discuss the temperature and hydraulic performance of the additional distribution layer in cooler design 2, applied on the lidless package. The temperature distribution for the improved design is measured for different flow rates, from 0.5 to 3.25 LPM, and compared with the reference cooler in Fig. 12. The temperature profiles for design 1 show larger chip temperature gradients, especially for a low flow rate of 0.5 LPM, whereas the temperature distribution for design 2 is more uniform. This is due to the more uniform inlet nozzle flow distribution by using the additional manifold layer.

The thermal performance of the reference cooler (design 1) and the cooler with the additional distribution layer (design 2) is compared in Fig. 13, in terms of the average chip temperature and the temperature gradient. This temperature gradient is defined as the difference between the maximum and minimum chip temperatures.

In general, the average chip temperature is slightly higher for cooler design 2. Except for the flow rate of 0.5 LPM, a significant reduction of the chip temperature of 20% is measured. This is because uniform flow distribution can improve the heat spreading through the bottom substrate package. With respect to the chip temperature uniformity, it can be observed that design 2 achieves a lower chip temperature gradient. Compared to the reference design, the chip temperature gradient is reduced by a factor of 4 and 2.3 for the flow rate values of 0.5 and 3 LPM, respectively. Moreover, the pressure drop is measured between the inlet and outlet tube connectors. The pressure measurements show that despite the presence of the additional distribution layer in the cooler, the impact on the measured overall pressure drop is insignificant.

C. High Power 1-kW Measurement

In the previous section, the cooler has been characterized for an applied chip power of 276 W, where a very low chip temperature can be achieved. Therefore, there is a lot of potentials to further increase the power. In this section, the applied power is increased to 1 kW. The applied voltage to the test board is 99 V, which is limited by the 10-A current limit of voltage source. The actual measured dissipated power in the heaters of the test chip is 935 W, corresponding to a chip power density of 175 W/cm^2. The measurement results for the vertical cooler design with 2-mm nozzle pitch are shown in Fig. 14. It shows that the measured chip temperature increase is ~65 °C for a flow rate of 3 LPM. Moreover, the coolant

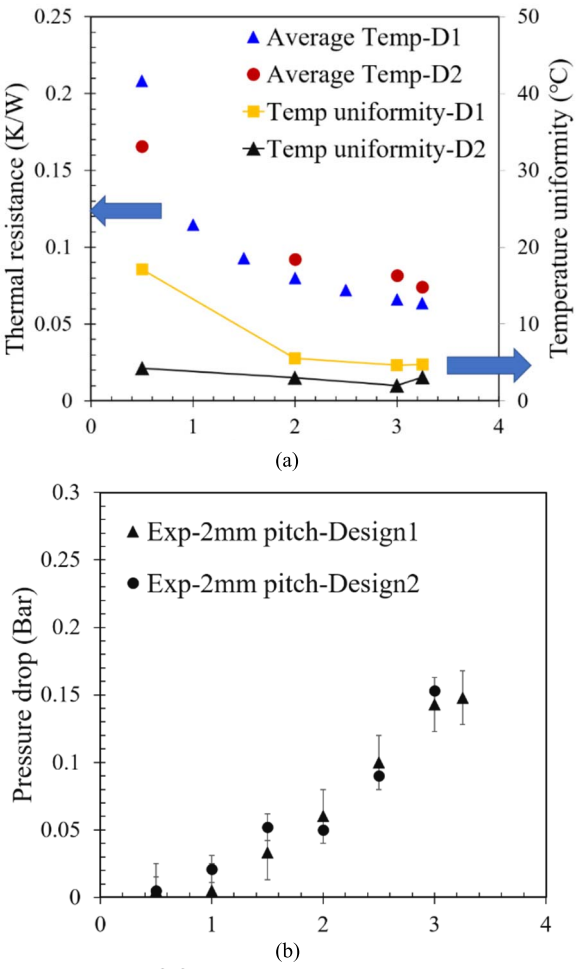

Fig. 13. Thermal and hydraulic comparison between designs 1 and 2. (a) Thermal resistance based on averaged chip temperature and temperature uniformity comparison. (b) Pressure drop comparison (applied voltage 50 V).

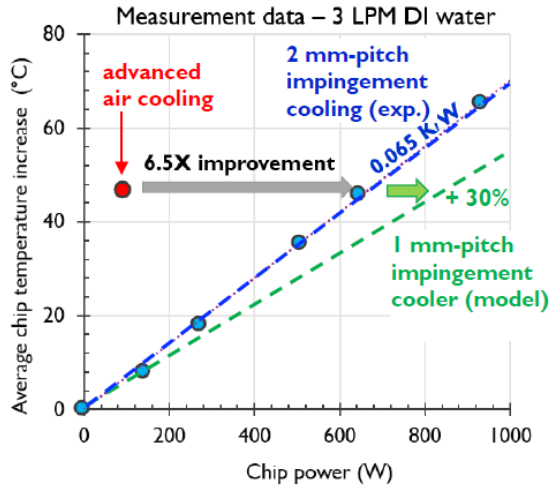

Fig. 14. High-power measurement with 1 kW for 2-mm inlet nozzle pitch (FL = 3 LPM, Re = 872, H/D = 1, and P/D = 3.33).

temperature increase is 4.5 °C. The average thermal resistance of the cooling with 3 LPM is 0.065 K/W, which is a 6.5 times reduction compared with the standard air cooling of the same chip package [22]. In addition, the temperature results show a linear temperature increase versus chip power, indicating a constant cooling performance of the cooler. The cooling

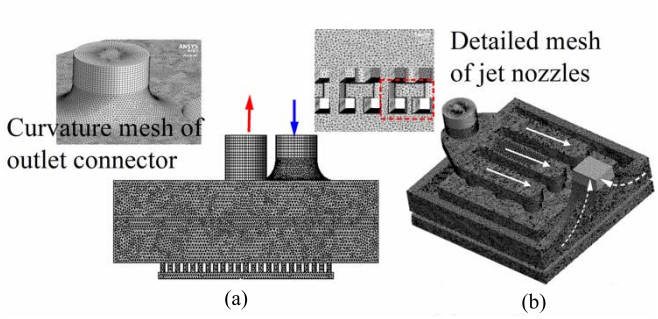

Fig. 15. Meshing details of the CFD models for the two cooler configurations. (a) Design 1. (b) Design 2.

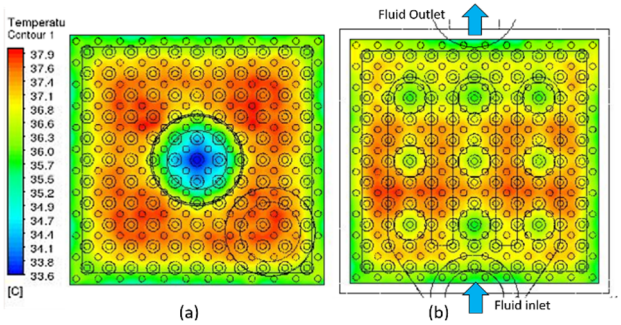

Fig. 16. Temperature distribution comparison with CFD modeling results: design 2 with additional distribution layer shows better temperature uniformity. (a) Design 1. (b) Design 2. FL = 3 LPM, heat flux = 100 W/cm^2, Re = 872, H/D = 1, and P/D = 3.33.

performance can be further improved by reducing the nozzle pitch (1-mm pitch), based on our previous nozzle scaling study [23], where it was shown that a nozzle unit cell computation fluid dynamic (CFD) model can be used to predict the average cooling performance. The blue curve in Fig. 14 shows a good agreement between the unit cell model and the measurement data for 2-mm nozzle pitch cooler. The unit cell model for 1-mm pitch predicts a further 30% performance improvement compared to the 2-mm nozzle pitch cooler for the same flow rate. In Section V, a full-scale CFD model will be performed to investigate the impact of the finer nozzle pitch on the temperature distribution of the chip and the cooler pressure drop.

V. Nozzle Pitch Impact Modeling Study

A. Modeling Methodology

Since the temperature gradient and nozzle flow rate uniformities are very important for the large die cooler design, a full cooler level, conjugated heat transfer fluid flow CFD model is used for the assessment. The CFD modeling is performed using ANSYS 18.0 software. First, the CFD model is validated for the two cooler designs with 2-mm nozzle pitch. Next, the validated CFD model is used to predict the thermal and hydraulic impact of the nozzle pitch reduction.

The extracted fluid domain from the computer-aided design (CAD) structure is shown in Fig. 15, where the solid domain of the cooler structure is excluded. Since the heat transfer is dominated by the convection in the liquid coolant, the impact of the conduction in the plastic cooler material is negligible and these parts can be omitted from the model [5]. The additional distribution layer can be seen clearly in

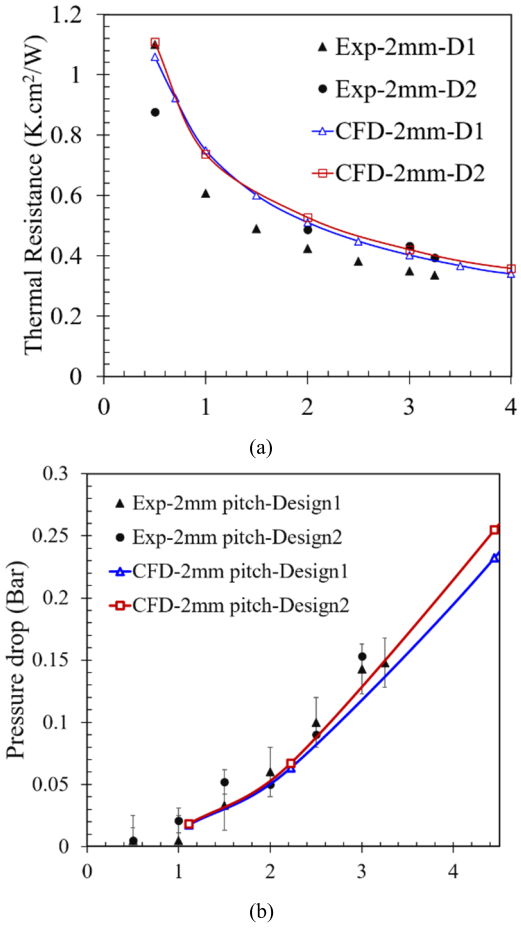

Fig. 17. Experimental validations of the CFD modeling results. (a) Averaged chip temperature validation. (b) Pressure drop between inlet and outlet.

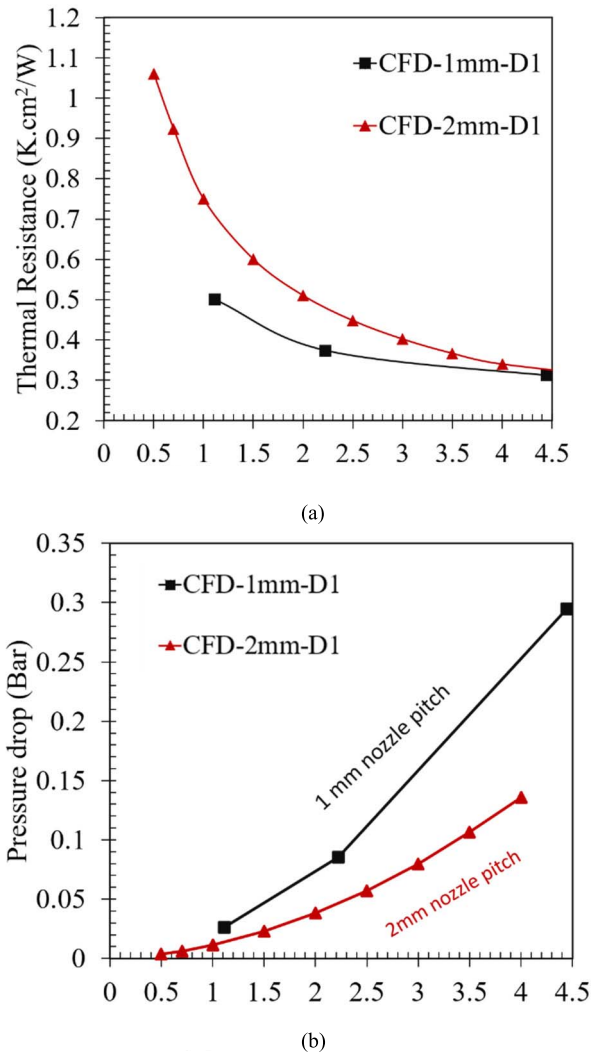

Fig. 18. (a) Temperature distribution and (b) pressure drop comparison with CFD modeling results: for nozzle pitch of 2 and 1 mm (heat flux = 100 W/cm^2).

Fig. 15(b), whereas the vertical design cooler is shown in Fig. 15(a). The minimum element size in the fluid domain is determined by the nozzle diameter (0.6 mm). Therefore, the minimal mesh size of the fluid domain is set at 0.1 mm, resulting in six mesh cells inside the nozzle diameter. For the meshing of the boundary layer, the first layer thickness is set as 1 μm with a growth ratio of 1.5. The minimal mesh size of the solid chip part is 0.01 mm. The meshing details for designs 1 and 2 are shown in Table III. Since the full-scale CFD model of the considered coolers is a scaled version of the smaller die size cooler with the same nozzle dimensions and nozzle to chip surface distance, just with a larger nozzle array, the results of the mesh sensitivity study for the small size cooler [23] also apply for this large die size cooler. The mesh sensitivity study showed that the results for the average chip temperature and the stagnation chip temperature can be considered mesh independent with a truncation error of 0.3% and a grid convergence index (CGI) of 0.03 for the considered element sizes.

For the numerical modeling scheme, the SemiImplicit Method for Pressure-Linked Equations (SIMPLE) algorithm is used as the solution method, whereas the Quadratic Interpolation for Convective Kinetics (QUICK) scheme is chosen for the numerical discretization. The convergence criteria were set at 10^{-5} for continuity, 10^{-6} for energy, and 10^{-6} for k, ω, and momentum (x, y, and z components of velocity) equations, respectively. A transition shear stress transport (SST) turbulence model has been used to predict the flow behavior covering laminar, turbulent, or in the transition regime in the different parts of the cooler. Our previous study [24] on a similar geometry showed that the SST model can predict the stagnation Nusselt number and the average Nusselt number, as well as the local-level pressure coefficient f with less than 5% difference in the range of $30 < \mathrm{Re_d} < 4000$, compared with a reference large eddy simulation (LES) model.

B. Modeling Validations

The modeling results for the chip temperature distribution for both cooler designs are shown in Fig. 16. The CFD modeling results show that the introduction of the distribution layer in design 2 results in a more uniform temperature distribution compared to design 1. The coldest region for design 1 is located in the chip center, which corresponds to the

TABLE III
MESHING COMPARISON BETWEEN DESIGNS 1 AND 2

	Design 1	**Design 2**
Fluid domain	0.1 mm	0.1 mm
First layer thickness	1e-3 mm	1e-3 mm
Layer number	10	10
Growth ratio	1.5	1.5
Total element size	18,279,453	15,201,961

central vertical feeding zone. This effect can be successfully reduced by adding an extra distribution layer, as shown in Fig. 16(b).

Fig. 17(a) shows the normalized thermal resistance comparison based on the average chip temperature, comparing the measurement data (dots) and the modeling results (solid lines). In general, the CFD model overpredicts the average chip temperature for design 1, especially for low flow rate values below 2 LPM. The small difference can be attributed to the simplification of the CFD model, where chip package below the Si chip has been replaced by an equivalent boundary condition. The thermal spreading in the chip package can result in a reduction of the chip temperature, especially at low flow rates. However, at higher flow rates, the difference between experiments and CFD modeling becomes smaller, as the significance of the downward thermal path through the package reduces as the convection on the chip surface by jet impingement cooling increases. At the target flow rate of 3 LPM, the difference between the CFD model and the experiment is as small as 14.2%.

Fig. 17(b) shows the pressure drop comparison between the experiments and modeling data for different flow rates. The pressure measurements show that the impact on the measured overall pressure drop is insignificant. These measurement results prove that the unique fabrication capabilities of additive manufacturing enable the design and fabrication of better large die coolers resulting in more uniform coolant flow distribution and temperature distribution. The pressure drop caused by the additional required layers is insignificant.

C. Nozzle Pitch Impact

The validated CFD modeling methodology is applied to the full-scale model with 1-mm pitch. The simulated thermal resistance and pressure drop for 2-mm nozzle pitch and 1-mm nozzle pitch are compared in Fig. 18. The number of nozzles increases from 121 for the 2-mm case to 484 for the 1-mm case. Moreover, the nozzle diameter changes from 0.6 mm for the 2-mm case to 0.3 mm for the 1-mm case. For a flow rate of 3 L/min, this will cause the Reynolds number to drop from 872 to 436. The modeling results show that the finer nozzle pitch can achieve 15.4% lower thermal resistance compared with the 2-mm pitch in the relevant flow rate range to 3 LPM. The detailed CFD model, which includes all details of the cooler and considers the flow distribution in the manifold and the temperature distribution in the chip, thus shows that the reduction of the nozzle pitch improves the cooler thermal performance. This happens, however, at the expense of an increased pressure drop over the cooler and, consequently, an increased pumping power. Fig. 18(b) shows that the cooler pressure drop increases by a factor of 1.92, as the nozzle pitch reduces by half for a constant flow rate of 3 LPM.

VI. CONCLUSION

In this article, we designed, fabricated, and characterized a package-level 3-D printed multijet cooler with sub-mm microjets, applied to a 23 × 23 mm^2 large die with almost 1000-W power dissipation. The reached power dissipation density is around 175 W/cm^2. For a coolant flow rate of 3 LPM, the average chip temperature increase is 65 °C with a pressure drop of 0.15 bar between the cooler inlet and the outlet. This low-pressure drop can highly reduce the required system pump power. At that flow rate, the cooling on the bare die outperforms the cooling on the lidded package by 35%. The temperature nonuniformity is investigated in detail, which shows that there is a significant impact from the coolant flow distribution. Compared to the reference design, the introduction of an additional distribution layer reduces the chip temperature gradient by a factor of 4 and 2.3 for flow rate values of 0.5 and 3 LPM, respectively.

Moreover, it is demonstrated that additive manufacturing enables the accurate fabrication of complex internal structures in multiple layers inside the 3-D printed large die cooler as one single piece, allowing the creation of additional structures to improve the flow and temperature uniformity without significant increase of the pressure drop over the cooler. The nozzle pitch impact modeling study indicates that finer nozzle pitch can achieve lower thermal resistance, however, at a penalty of the increase of pressure drop. For the outlook of this article, the investigation of the reliability for the 3-D printed cooler material is valuable for the cooler designers. Also, hot spot cooling with different heat flux patterns will be studied, which is more realistic in real applications.

REFERENCES

[1] D. B. Tuckerman and R. F. W. Pease, "High-performance heat sinking for VLSI," *IEEE Electron Device Lett.*, vol. LED-2, no. 5, pp. 126–129, May 1981.
[2] T. Wei, "All-in-one design integrates microfluidic cooling into electronic chips," *Nature*, vol. 585, no. 7824, pp. 188–189, 2020.
[3] T. W. Wei, H. Oprins, V. Cherman, E. Beyne, and M. Baelmans, "Experimental and numerical investigation of direct liquid jet impinging cooling using 3D printed manifolds on lidded and lidless packages for 2.5D integrated systems," *Appl. Thermal Eng.*, vol. 164, Jan. 2020, Art. no. 114535.
[4] T. Brunschwiler *et al.*, "Direct liquid jet-impingment cooling with micron-sized nozzle array and distributed return architecture," in *Proc. Thermal Thermomech, 10th Intersoc. Conf. Phenomena Electron. Syst.*, Jun. 2006, pp. 196–203.
[5] T. Tiwei *et al.*, "High efficiency direct liquid jet impingement cooling of high power devices using a 3D-shaped polymer cooler," in *IEDM Tech. Dig.*, Dec. 2017, pp. 32.5.1–32.5.4.
[6] T.-W. Wei *et al.*, "Experimental characterization and model validation of liquid jet impingement cooling using a high spatial resolution and programmable thermal test chip," *Appl. Thermal Eng.*, vol. 152, pp. 308–318, Apr. 2019.
[7] T. Wei *et al.*, "Experimental characterization of a chip-level 3-D printed microjet liquid impingement cooler for high-performance systems," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 9, no. 9, pp. 1815–1824, Sep. 2019.

[8] H. El-Aawar, "Increasing the transistor count by constructing a two-layer crystal square on a single chip," *Int. J. Comput. Sci. Inf. Technol.*, vol. 7, no. 3, pp. 97–105, 2015.
[9] J. Hruska. (Aug. 21, 2019). *Intel Details Its Nervana Inference and Training AI Cards*. [Online]. Available: https://www.extremetech.com/computing/296990-intel-nervana-nnp-i-nnp-t-a-training-inference
[10] (2019). *Reaching New Heights With the World's Largest FPGA*. [Online]. Available: https://www.xilinx.com/products/silicon-devices/fpga/virtex-ultrascale-plus-vu19p.html#advantage
[11] (2019). *Nervana Neural Network Processor—Intel AI*. [Online]. Available: https://www.intel.ai/nervana-nnp/
[12] (2019). *AMD EPYC 760*. [Online]. Available: https://www.amd.com/en/products/cpu/amd-epyc-7601
[13] (2019). *CS-1 is Powered by the Cerebras Wafer Scale Engine—The Largest Chip Ever Built*. [Online]. Available: https://www.cerebras.net/
[14] (2019). *IBM Z15 (8561) Technical Guide*. [Online]. Available: https://www.redbooks.ibm.com/redpieces/pdfs/sg248851.pdf
[15] *DSMSomosWaterShed11122*. Accessed: 2015. [Online]. Available: https://www.protolabs.co.uk/media/1010047/somos-watershed-en.pdf
[16] O. K. Siddiqui and M. S. Zubair, "Efficient energy utilization through proper design of microchannel heat exchanger manifolds: A comprehensive review," *Renew. Sustain. Energy Rev.*, vol. 74, pp. 969–1002, Jul. 2017.
[17] H. Liu, P. Li, and J. Van Lew, "CFD study on flow distribution uniformity in fuel distributors having multiple structural bifurcations of flow channels," *Int. J. Hydrogen Energy*, vol. 35, no. 17, pp. 9186–9198, Sep. 2010.
[18] C. U. Gonzalez-Valle, S. Samir, and B. Ramos-Alvarado, "Experimental investigation of the cooling performance of 3-D printed hybrid water-cooled heat sinks," *Appl. Thermal Eng.*, vol. 168, Mar. 2020, Art. no. 114823.
[19] L. E. Paniagua-Guerra, S. Sehgal, C. U. Gonzalez-Valle, and B. Ramos-Alvarado, "Fractal channel manifolds for microjet liquid-cooled heat sinks," *Int. J. Heat Mass Transf.*, vol. 138, pp. 257–266, Aug. 2019.
[20] L. E. Paniagua-Guerra and B. Ramos-Alvarado, "Efficient hybrid microjet liquid cooled heat sinks made of photopolymer resin: Thermofluid characteristics and entropy generation analysis," *Int. J. Heat Mass Transf.*, vol. 146, Jan. 2020, Art. no. 118844.
[21] T. Borrvall and J. Petersson, "Topology optimization of fluids in Stokes flow," *Int. J. Numer. Methods Fluids*, vol. 41, no. 1, pp. 77–107, 2003, doi: 10.1002/fld.426.
[22] T.-W. Wei *et al.*, "Demonstration of package level 3D-printed direct jet impingement cooling applied to high power, large die applications," in *Proc. IEEE 70th Electron. Compon. Technol. Conf. (ECTC)*, Jun. 2020, pp. 1422–1429.
[23] T. W. Wei *et al.*, "Nozzle scaling effects for the thermohydraulic performance of microjet impingement cooling with distributed returns," *Appl. Thermal Eng.*, vol. 180, Nov. 2020, Art. no. 115767.
[24] T. Wei, H. Oprins, V. Cherman, E. Beyne, and M. Baelmans, "Conjugate heat transfer and fluid flow modeling for liquid microjet impingement cooling with alternating feeding and draining channels," *Fluids*, vol. 4, no. 3, p. 145, 2019.

Tiwei Wei (Member, IEEE) received the Ph.D. degree from the Interuniversity Microelectronics Centre (imec), Leuven, Belgium, and KU Leuven, Leuven, in 2020.

He worked as a Research Staff with Tsinghua University, Beijing, China, and The Hong Kong University of Science and Technology, Hong Kong, from 2011 to 2015, where he worked on advanced microelectronic packaging techniques. He joined imec in 2015, starting the Ph.D. research with developing electronic cooling solutions for high-performance systems. He is currently a Post-Doctoral Research Scholar of Mechanical Engineering with Stanford University, Stanford, CA, USA. His current research interests include impingement jet cooling and embedded microchannel cooling for high heat flux applications.

Dr. Wei received the Imec Excellence PhD Award in 2020, Belgium FWO Fellowship in 2019, the EPS/ECTC 2019 Student Travel Award (ten recipients), and ITherm 2019 Student Travel Grant.

Herman Oprins (Member, IEEE) received the M.Sc. and Ph.D. degrees in mechanical engineering from Katholieke Universiteit (KU) Leuven, Leuven, Belgium, in 2003 and 2010, respectively.

He joined imec, Leuven, in 2003, where he has been involved in thermal experimental characterization, thermal modeling, and thermal management solutions, where he is currently a Principal Member of Technical Staff and a Research and Development Team Leader. His research interests include the thermal analysis and thermal solutions for advanced chip packages, 3-D ICs, back end of line stacks, silicon photonics, GaN transistors, photovoltaic modules, and microfluidics.

Vladimir Cherman (Member, IEEE) received the M.Sc. and Ph.D. degrees in electronic engineering from Saint-Petersburg Electrotechnical University (ELTECH), Russia, in 1994 and 1999, respectively.

From 1997 to 2000, he was an Electronics Engineer with Morion Inc., St Petersburg, Russia. From 2000 to 2007, he was with the Ceramics Laboratory, Swiss Federal Institute of Technology Lausanne (EPFL), Lausanne, Switzerland, where his research was focused on microwave properties and applications of ferroelectric materials. He joined the Reliability and Modeling Group, IMEC, Leuven, Belgium, as a Researcher, in 2007, where he is involved in the study of chip package interaction (CPI) and reliability of 3-D integration solutions and electronic packages.

Zhi Yang received the B.S. and Ph.D. degrees from the Mechanical Engineering Department, University of Maryland, College Park, MD, USA, in 2012 and 2017, respectively.

Since 2018, he has been working as a Sr. Thermal and Packaging Engineer with GlobalFoundries, Malta, NY, USA. He specializes in thermal and mechanical design and optimization for consumer electronic packages and medical devices. He has coauthored more than 30 technical journal articles and conference articles with total citations of over 2400. His research includes numerical analysis and modeling, material characterization, and 2.5-D/3-D IC packaging.

Kathryn C. Rivera received the M.S. degree from the Mechanical Engineering Department, Rensselaer Polytechnic Institute, Troy, NY, USA, in 1993.

She is currently a Sr. Principal Engineer of Mechanical with Northrop Grumman, Baltimore, MD, USA. She is a semiconductor thermal packaging expert skilled in developing, simulating, and validating electronic package designs. She has strong experience in the areas of packaging materials, thermal performance characterization, product development, supplier/project management, and root cause/failure analysis.

Geert Van der Plas (Member, IEEE) received the Ph.D. degree from Katholieke Universiteit Leuven, Leuven, Belgium, in 2000.

In 2003, he joined imec, Leuven. He has been working on energy-efficient data converter, power/signal integrity, and 3-D integration technologies. He is currently a Scientific Director and a Program Manager in the 3-D program addressing system scaling using advanced 3-D [through silicon via (TSV)] and packaging [fan-out wafer-level packaging (FO-WLP)] technology for high-performance, mobile, and Internet of Things (IoT) applications. His research interests are in characterization, modeling, system exploration, and design enablement of 3-D integration technologies.

Bartlomiej J. Pawlak received the M.S. degree in physics from the University of Warsaw, Warsaw, Poland, in 1996, and the Ph.D. degree from the University of Amsterdam, Amsterdam, The Netherlands, in 2001, with research focusing on optically active defects in silicon.

Since 2001, he has been a Senior Scientist with Philips Research Leuven, Leuven, Belgium, studying doping technologies for advanced CMOS devices in digital applications. He is currently with GlobalFoundries, IMEC, Leuven.

Luke England received the B.S. degree in materials engineering and the M.S. degree in materials science and engineering from Iowa State University, Ames, IA, USA, in 2002 and 2004, respectively.

He has developed packaging technologies encompassing a wide range of disciplines for companies including Micron Technology, San Jose, CA, USA, and Fairchild Semiconductor, Sunnyvale, CA, USA. In 2012, he began working for GlobalFoundries, Malta, NY, USA, as an on-site assignee to IMEC, Leuven, Belgium, as part of the 3-D development program, where his responsibility is leading the through silicon via (TSV) and 3-D Packaging Development Team. He is currently a Packaging Technologist with Marvell Semiconductor, East Fishkill, NY, USA.

Eric Beyne (Senior Member, IEEE) received the master's degree in electrical engineering and the Ph.D. degree in applied sciences from KU Leuven, Leuven, Belgium, in 1983 and 1990, respectively.

He has been with imec, Leuven, since 1986, where he has been involved in advanced packaging and 3-D interconnect technologies. He is currently the imec Senior Fellow, a VP Research and Development, and the Program Director of imec's 3-D System Integration Program.

Martine Baelmans received the Ph.D. degree in engineering from KU Leuven, Leuven, Belgium, in 1993.

She is currently a Professor with the Department of Mechanical Engineering, KU Leuven, where she has been leading the Group on Thermal-Fluid Engineering, since 1996. She has authored or coauthored more than 200 articles in applications on fluid mechanics and heat transfer. Research topics are presently focusing on automated optimization in thermal design. Starting from dedicated component and system models, parameters, shapes, and topologies are improved. Applications range from liquid and two-phase cooling over thermal management in power electronics, power transformers, and energy systems.