Copper Filling Process for Small Diameter, High Aspect Ratio Through Silicon Via (TSV)

Tiwei Wei[1], Jian Cai[1,2,*], Qian Wang[1], Ziyu Liu[1], Yinan Li[3], Tao Wang[1], Dejun Wang[3]
[1]Institute of Microelectronics, Tsinghua University, Beijing 100084, P. R. China
[2]Tsinghua National Laboratory for Information Science and Technology, Beijing 100084, P. R. China
[3]Faculty of Electronic information and Electrical Engineering, Dalian University of Technology, Dalian 116024, P. R. China
*Email: jamescai@tsinghua.edu.cn

Abstract

3D Integration is a good solution for extending Moore's momentum in the next decennium. Through Silicon Via (TSV) is an alternative interconnect technology for higher performance system integration with vertical stacking of chips in package. Due to high demands of chip miniaturization, small diameter TSV with high aspect ratio has become particularly important.

This paper focuses on Cu electroplating via filling of small diameter, high aspect ratio TSV. Samples of different via diameters under various current densities are fabricated and analyzed in lab. In addition, exhaust and pre-wetting procedures are also introduced after a series of contrast experiments, robust copper filling result for small diameter (4μm ~6μm) TSVs with high aspect ratio up to 6:1 has been successfully realized. Based on the good copper filling result, a testing vehicle structure of 3D integration is fabricated.

1. Introduction

With rapid development of semiconductor technology, traditional 2D integration was unable to meet the demands of light, thin, short and small in consumer electronic products, such as cellular phones, tablet PCs, smartphones and so on. Within this circumstance, 3D integration technology is attracting more and more attention because of its performance, size and cost advantages for a very wide range of applications. Especially, 3D integration provides new architectures for sophisticated ICs and facilitates the integration of heterogeneous materials, devices, and signals, enabling the realization of extended System-On-Chip (SOC)[1,2,3].

Among all kinds of 3D packaging techniques, TSV technology is an important interconnect technology for higher performance system integration with vertical stacking of chips in package[4]. TSV can achieve smaller delay and power consumption, heterogeneous integration with potentially lower cost and time-to-market. Via formation, filling and temporary bonding of wafers are key issues for 3D integration with TSV.

Copper is regarded as one of the most widely used conductive materials to fill the vias due to its low electrical resistance, compatibility to conventional multilayer interconnections, and relatively good match to silicon's coefficient of thermal expansion[5]. Electroplating technology is considered to be the most suitable for copper filling of TSV[6], which can be realized by either through vias or blind vias[7]. However, copper filling process of small diameter with high aspect ratio TSV is challenging with conventional damascene copper electroplating technology. For example, it is difficult to form a uniform and continuous seed layer inside higher aspect ratio vias by traditional sputtering process since the film thickness at the sidewall is much smaller than that of the surface[8]. Another fatal defect for TSV is the voids inside the filled via during plating.

Several approaches related to copper electroplating have been developed to solve problems mentioned, such as reverse pulse waveform, optimization of electroplating bath and current density solution[3,9,10]. Although great progress has been achieved, copper filling for small diameter and high aspect ratio TSV still faces a lot of problems to realize robust copper.

This paper would focus on via filling process for small diameter, high aspect ratio TSV. To realize robust copper electroplating process for small diameter (4μm ~6μm) TSVs with high aspect ratio up to 6:1, exhaust and pre-wetting process are firstly introduced, and also current density optimization is studied in this paper. This paper also investigates the voids in copper via filling. Through a series of contrast experiments, the vias are filled by damascene copper electroplating process with high aspect ratio.

After copper filling process, thick surface copper above the wafer can be removed by CMP(Chemical Mechanical Polishing). Besides, backside wafer thinning process and fabrication of RDL are achieved by introduction of temporary transfer wafer which can provide mechanical support to the device wafer.

2. Copper filling process

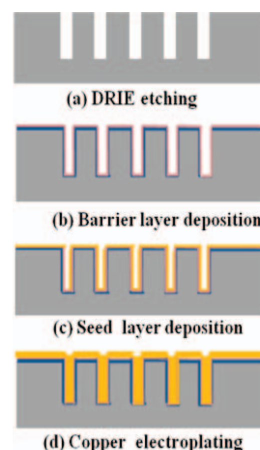

Fig. 1 Copper filling process of TSV

A typical TSV process is shown in Fig.1, including DRIE etching, barrier layer/seed layer deposition and Cu plating. Blind via formation is adopted in this process. Designed TSVs with different via sizes and aspect ratios are fabricated with this process.

2.1 Formation of blind vias

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During the formation of blind vias , DRIE etching process from (Surface Technology System) STS exhibits selectivity between silicon and the photoresist used as masking material, and Bosch etching mechanism is adopted in the STS DRIE etcher.

Fig.2 shows the alternating etching and passivation cycles in Bosch process, which is based on successive cycling of SF_6+O_2 etch and C_4F_8 passivation gases[11].

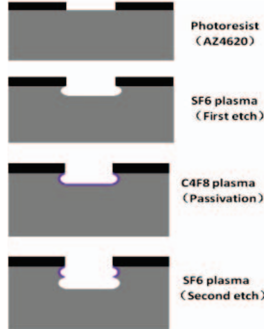

Fig 2 Bosch process for high aspect ratio TSV

In Bosch DRIE process, SF_6 is used to etch Si substrate at first, and then C_4F_8 is used to deposit substrate. Addition of O_2 to these gases can help to control etch rate and selectivity. The cyclic nature of the Bosch process forms an undulating etched sidewall , which can be seen clearly in Fig.3.

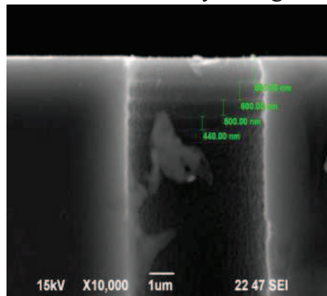

Fig.3 SEM image of undulating etched sidewall

In order to get high aspect ratio vias with vertical sidewall, 3s passivation cycle times and 5s etching cycle times are controlled by repeated etch and passivation steps. The Bosch process parameters were optimized as follows: RF power of 1500W/800W; SF_6 flow rate of 280 sccm; C_4F_8 flow rate of 80 sccm; O_2 flow rate of 28 sccm and the platen power of 42W.

Then continuous barrier and seed layers will be realized on vertical sidewall by via lining process respectively. Thermal oxidation is utilized to deposit the insulating layer(500nm SiO_2) on sidewall of the vias, and the barrier and seed layers with 200nm TiW/ 500nm Cu are obtained by magnetron sputtering, as shown in Fig.4.

Fig.4 Seed layer deposition with 4.5μm diameter and 40μm depth TSV

2.2 Copper electroplating

There are several factors with wafers during via filling, such as via density, via diameter, etc[12]. Exhaust and pre-wetting process are extremely important [13]. Ultrasonic pre-wetting is applied to break the air bubbles inside the via. With this method, air bubbles can be released from the via much easily .

(a) Effect of Pre-wetting

Shown in Fig.5 is one of the FIB images of high aspect ratio vias. The via size is 5μm with a depth of 25μm. The plating is performed without pre-wetting.

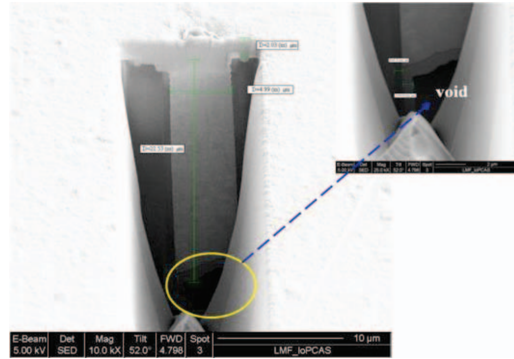

Fig. 5 Void in 5μm via diameter and 25μm depth TSV

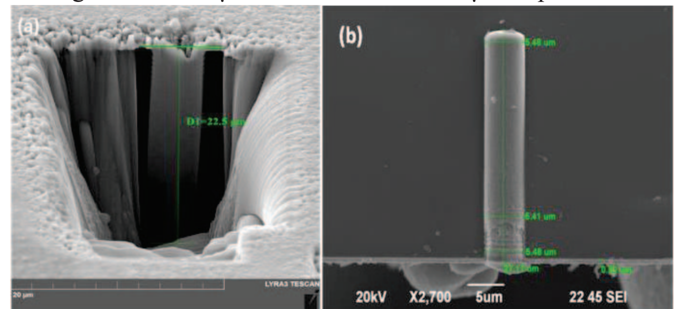

Fig.6 Void-free copper filling with pre-wetting (a)FIB image for 5μm via diameter and 25μm depth TSV;(b)SEM image for 5.5μm via diameter

In contrast, Fig.6 shows void-free copper filling for 5μm and 5.5μm via diameter with 25μm depth TSV after ultrasonic pre-wetting treatment. It is obviously that the void shown in Fig.5 is existed due to lack of chemistry at the bottom of via when plating started, and pre-wetting process can effectively solve the problem.

(b) Effect of Seed layers

As well known, it is difficult to get uniform and continuous films in higher aspect ratio vias through conventional sputtering process. In this paper, barrier and seed layers with 200nm TiW/500nm Cu are sputtered by Kurt Lesker Lab18 sputter systems. Different via diameters (4μm, 4.5μm, 5μm and 6μm) with 40μm depth TSVs are fabricated and analyzed in lab to compare step coverage result. Fig.7 shows TSV filling partition test at different via diameters with sputtered TiW/Cu seed layers.

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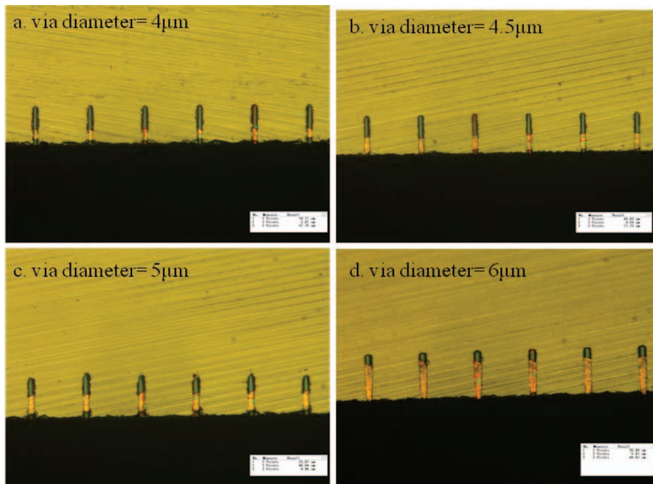
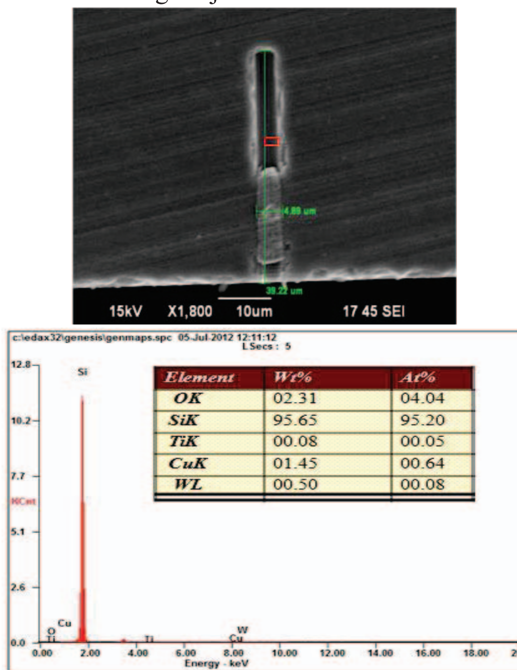


Fig.7 TSV filling partition test at different via diameters with sputtered TiW/Cu seed layers

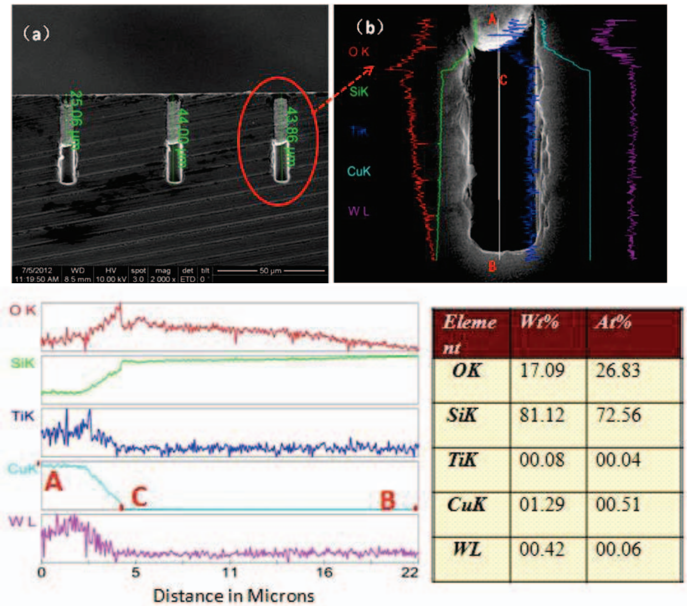
Seed layers under different via diameters are investigated through EDX(Energy Dispersive X-ray) analysis. Fig.8 shows seed layers analysis of 4.5μm diameter with 40μm depth through EDX. Poor seed layers can be seen at the range of 20μm height for 40μm depth TSV. The weight percent of Cu in red calibration range is just 1.45%.



Element	Wt%	At%
OK	02.31	04.04
SiK	95.65	95.20
TiK	00.08	00.05
CuK	01.45	00.64
WL	00.50	00.08

Fig.8 EDX analysis of 4.5μm diameter with 40μm depth

Fig.9(a) shows copper filling results of 5μm diameter with 40μm depth, and the upper 25μm of the vias are filled. Fig.9(b) shows seed layers distribution through EDX line scanning from point A to point B. With the increase of via depth, seed layers become less and less. The weight percent of Cu at the corner of point C is 1.29%.



Element	Wt%	At%
OK	17.09	26.83
SiK	81.12	72.56
TiK	00.08	00.04
CuK	01.29	00.51
WL	00.42	00.06

Fig.9 EDX analysis of 5μm diameter with 40μm depth

Based on the EDX analysis of seed layers, it can be seen that the smaller the TSV diameter is, the more difficult for seed layers sputtered. In Fig.7, voids were observed for different via diameters owing to insufficient coverage of seed layers at the via bottom. In conditions of the poor seed layers at the bottom of TSV(6μm diameter and 40μm depth), good copper fillings with high aspect ratio are realized, and the upper 36 μm of the vias are successfully filled.

(c) Effect of Current density

Current density is also an important affecting factor in copper electroplating. Samples under different current densities are also dicussed in this paper. When the current density increases, it will accelerate the current crowding at the via mouth, and also limit mass transfer at the via bottom.

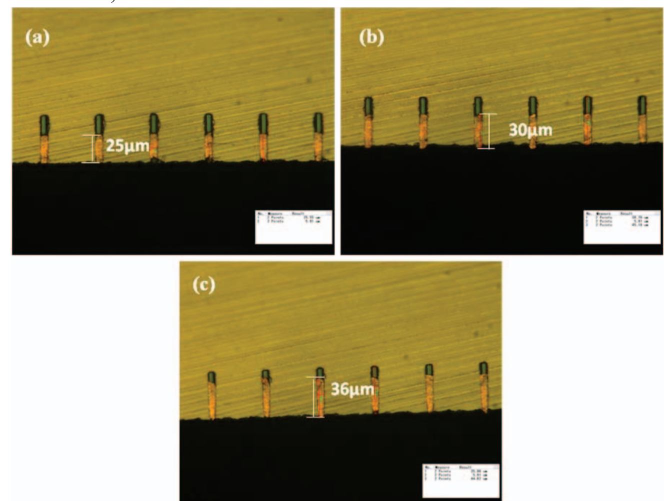


Fig.10 TSV(via diameter=6μm;via depth=40μm) plating with different current densities .(a)0.1ASD (b)0.08ASD(c)0.06ASD

Fig.10 shows the copper filling results under different electroplating current densities 0.1ASD, 0.08ASD, 0.06ASD , respectively, with 6μm via diameter and 40μm via depth. A conclusion can be made that low current density is more

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efficient to filling vias for small diameter and high aspect ratio TSV.

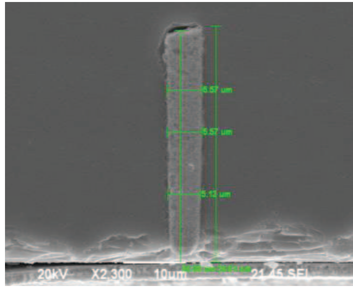

Fig. 11 Robust filling result with 5.5μm via diameter and 36μm depth TSV

As shown in Fig.11, robust copper electroplating result for small diameter (5.5μm) TSV with high aspect ratio up to 6:1 is achieved by regulating of current density and via depth and others.

3 3D integration process with Small Diameter, High Aspect Ratio TSV

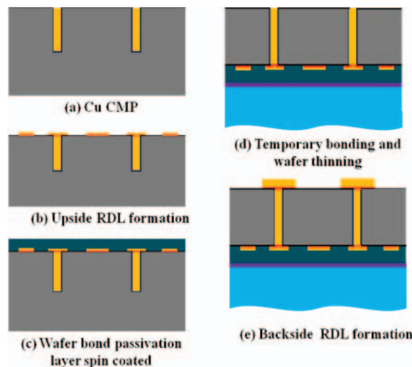

Fig.12 Fabrication process of small diameter, high aspect ratio TSV

Fig.12 shows the fabrication process of small diameter, high aspect ratio TSV which contains Cu CMP process , upside redistribution line(RDL) formation ,temporary bonding and wafer thinning and backside RDL formation.

Based on the robust copper filling process, thick surface copper above the wafer can be removed by CMP. After that, backside wafer thinning process and fabrication of RDL are made by use of temporary transfer wafer which can provide mechanical support to the device wafer.

Fig.13 shows a cross-section of testing structure with small diameter, high aspect ratio TSV. The testing structure was designed to investigate the reliability of TSVs through a daisy chain structure,which would be reported in other paper after full process development and integration.

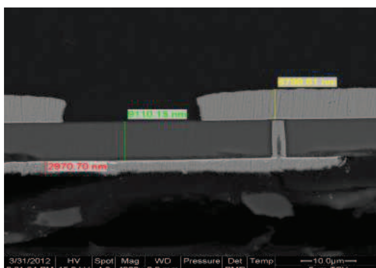

Fig.13 Cross-section of testing structure with small diameter, high aspect ratio TSV

Conclusions

In this paper, copper filling process for small diameter and high aspect ratio TSV has been investigated by optimization of the pre-wetting process and low current density. By use of the robust copper TSV, a testing vehicle structure of 3D integration based on high aspect ratio TSV is achieved.

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