A 3D Integration Testing Vehicle with TSV Interconnects

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Abstract

3D integration is one of the potential solutions for extending Moore's momentum in the next decennium. Through silicon via (TSV) is a key interconnect technology for future's higher performance and system integration with vertical stacked chips in package, which can achieve smaller interconnection delay, heterogeneous technologies integration and potentially lower cost and reduce time-to-market.

In this paper, a testing vehicle of 3D stacking dies with TSVs as the major interconnect was designed. A dummy die with 5μm diameter TSVs was fabricated and assembled on a silicon interposer, which has TSVs as well. The dummy die/chip was bonded on the interposer through Cu-Sn-Cu bonding at 280℃,and then, the bonded module was assembled on designed testing board.

Introduction

TSV fabrication technology and micro-bump interconnection between stacked dies are recognized as the core technologies of 3D integration. Lots of research works focusing on the fabrication and applications of difference size TSVs have been published from TSMC(Taiwan), IMEC(Europe), Samsung(Korea), Elpida(Japan), CEA-Leti(France), ITRI(Taiwan, China)[1] and many other research institutions all around the world.

However, there are still many challenges when facing fine pad pitch (50 μm) and small diameter(<10μm) TSV with high aspect ratio, such as wafer thinning and handling, alignment for warped wafers[2], dishing and uniformity, bottom up electroplating, the performance of insulating liner , assembly and interconnection with thin die. When the TSV diameter and depth becoming smaller, the problems mentioned above will be more and more evident. Via diameters smaller than 5μm are very difficult to be filled with electroplated copper[3]. Thin wafer handling is also the cornerstones of 3D stacked IC manufacturing, the quality of temporary bonding process becomes particularly important as the wafer thinned to 30μm and below. When the wafer thickness becomes thinner, the warpage will be more serious because of the stresses. Moreover, it is very challenge to align the warped wafers.

This paper focuses on the design and fabrication of a 3D integration testing vehicle, which includes design of 3D integration testing vehicle with 5μm TSVs, fabrication of test chip with 5μm TSVs and key technologies like via formation, copper electroplating, temporary bonding process, wafer thinning and polishing, alignment for warped wafers etc, fabrication of 40μm Si interposer, and assembly process.

Design of 3D Integration Testing Vehicle

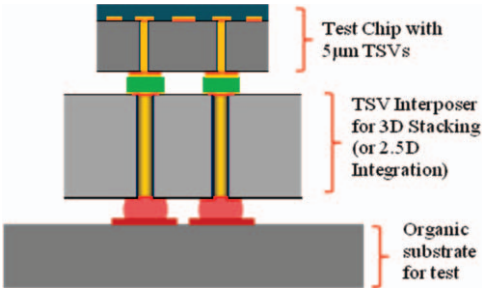

Fig.1 3D integration testing vehicle

Fig.1 shows the designed 3D packaging illustration enabled with small TSV (5μm) chip, TSV interposer chip and organic substrate.

As shown in the structure, the test chip with 5μm TSVs was bonded on the interposer through Cu-Sn-Cu bonding, and the size of Cu/Sn microbump is 60μm x 60μm, with 300μm pad pitch. Microbump layout was designed as mirror symmetrical with that of 5μm TSV chip. The size of test chip with 5μm TSVs is 6mm x 5mm, and the size of interposer with 40μm TSVs is 7mm x 6mm.

And then, the bonded module was assembled on a designed BT substrate with dimension of 8.5mm x7.5mm through solder ball. Pad size for solder ball placing is 100μm x 100μm, pad size of surrounding is 300μm x 300μm with a pad pitch of 500μm.

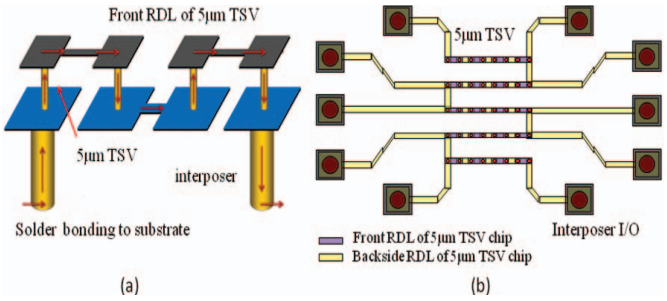

Fig.2 Daisy chain model (a) 3D view of TSV daisy chain model(b) Plane view of daisy chain

The designed daisy chain and Kelvin structure testing patterns are shown in Fig.2 and Fig.3. For the test chip with 5μm TSVs, the diameter of TSV is 5μm, and the chip thickness is 25μm which has the aspect ratio of 5:1. Daisy chain structure for successful interconnect verification and Kelvin structure for electrical resistance measurement were designed.

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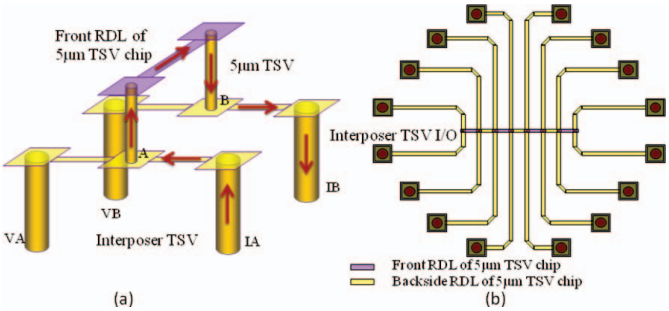


Fig.3 Kelvin structure model (a) 3D view of TSV Kelvin structure model(b) Plane view of Kelvin structure

Fabrication of Test Chip with 5μm TSVs

The dummy chip with 5μm TSVs was fabricated in-house. Fig.4 presents the fabrication process of 5μm TSV. The key processes of 5μm diameter and high aspect ratio TSV fabrication are TSV etching, lining and via filling, optimized temporary bonding/ debonding, wafer handling.

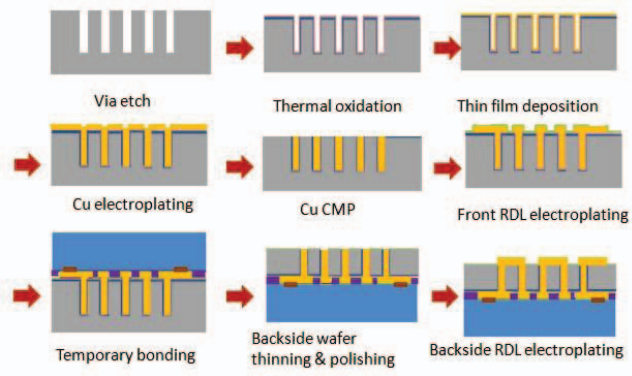


Fig.4 Process flow of test chip with 5μm TSVs

(A) Via filling of 5μm TSV

Photoresist was applied by lithography as mask of via formation. Deep Reactive Ion Etching (DRIE) process was used to form 5μm diameter blind via, with the height of 25μm. Bosch process was adopted with a STS DRIE etcher. After photoresist stripped, 500nm SiO_2 was formed through thermal oxidation, which was used as the insulating layer of 5μm TSV. And then, barrier and seed layers with 200nm TiW/500nm Cu were sputtered.

Based on the uniform and continuous seed layer inside 5μm diameter vias, robust copper electroplating process for 5μm TSVs with high aspect ratio was realized.

The 5μm TSV filling process was set up to adopt bottom-up Cu electroplating mechanism using electroplating chemicals from Shanghai Sinyang Semiconductor Materials Co., Ltd.

Current density is an important affecting factor in copper electroplating. Samples under different current densities were discussed in this paper. Low current density of 0.01ASD was used to fill the 5μm TSV for 16 hours with high aspect ratio up to 7:1, but it will take a lot of time. Voids at the bottom of the 5μm TSV were found as the current density was 0.1ASD. Finally, high current density of 0.25ASD was adopted as the optimized plating parameters of 5μm TSV Cu filling. The electroplating parameters of 5μm TSV are shown in Table.1.

Table.1 Optimized plating parameters of 5μm TSV Cu filling

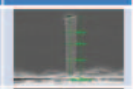
Condition	Current density	Electroplating time	Results
1	0.01ASD	16hour	
2	0.1ASD	3hour	
3	0.25ASD	25min	

Fig.5 presents a cross-sectional view of bottom-up electroplated TSV. From the SEM images, the insulating layer/ barrier and seed layers can be seen clearly, and via filling is void free.

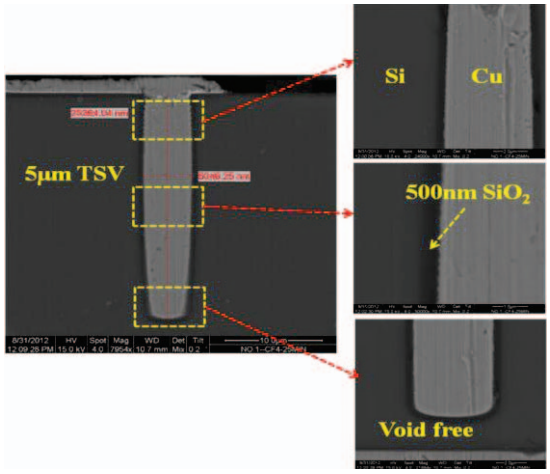


Fig.5 SEM images of 5μm TSV with upside pad

Subsequent copper chemical mechanical polishing (CMP) process was applied to remove Cu overburden on wafer surface, which could ensure copper planarization for wafer thinning and handling. According to the Cu CMP parameters reported in other paper[4], less overburden on wafer surface could be removed by CMP much more efficiently.

(B) Temporary bonding and wafer thinning

Temporary bonding was achieved through WaferBOND™ HT-10.10 using SUSS CB6L wafer bonder. The quality of temporary bonding was very important to attain better wafer thinning especially for test chip with 5μm TSVs.

Fig.6 presents the cross-section of 5μm temporary bonding, the thickness of WaferBOND™ is 5μm, and the thickness of the front RDL is 3μm. There are no bubble and crack in wafer bond and other interfaces.

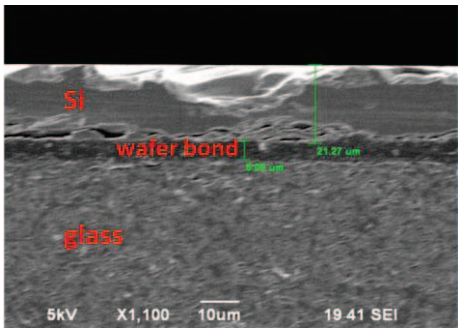


Fig.6 Cross-section of 5μm temporary bonding

Based on the good temporary bonding results, the backside wafer grinding/polishing process was applied to expose 5μm Cu TSV backside.

For goal thickness of 25μm, silicon wafer with 5μm TSVs was grinded down to 40μm at high speed of 0.2μm/s, and then the wafer with 40μm thickness was grinded down to 30μm at low speed of 0.1μm/s. At that time, polishing was applied to reduce the extra 5μm and meanwhile relieve the stress of grinding. Fig.7(a) shows the picture of a temporary bonded silicon wafer with 5μm TSVs, which has a thickness of 25μm. Fig.7(b) and (c) shows the surface with exposed 5μm TSVs after back grinding and polishing.

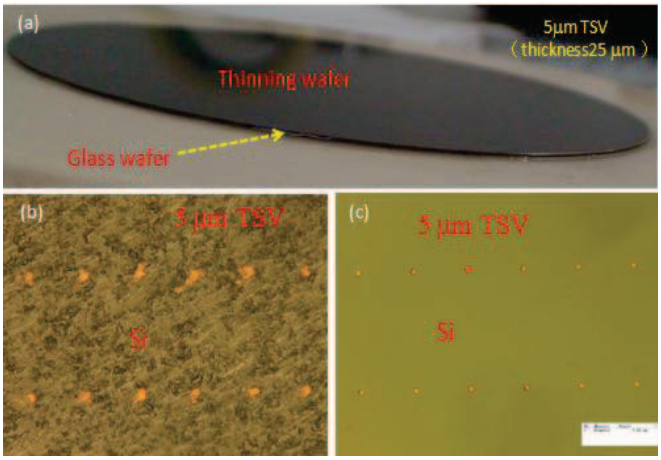


Fig.7 The surface of back grinding and polishing
(a)The picture of a temporary bonded silicon wafer with 5μm TSVs (b) The surface after back grinding (c) The surface after back polishing

(C) Microbump fabrication

After the 5μm Cu TSVs backside were exposed, 200nm SiO_2 passivation layer was deposited through PECVD at the temperature of 200℃. Because the wafer bond can't survival during high temperature, the process temperature after temporary bonding should be controlled under 220℃. Later, the third photolithography was used for defining Ohmic contact area, where SiO_2 passivation layer was etched. The quality of the back RIE process was crucial to electrical testing, and the alignment for opening passivation area of 5μm TSV was very difficult due to the warpage of thinned wafer. Good temporary bonding and enough polishing after wafer thinning would minimize the stress and warpage.

Fig.8 shows the cross-section of 5μm TSV daisy chain structure with good TSV filled.

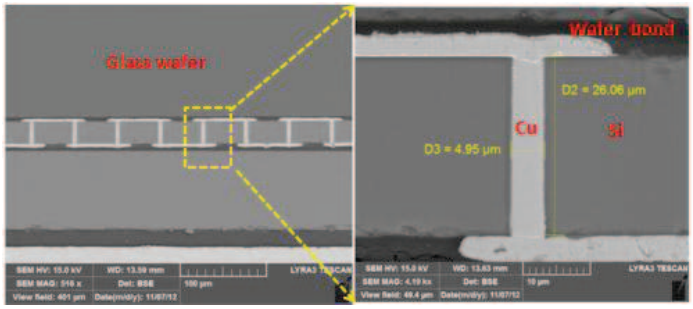


Fig.8 Cross-section of 5μm TSV daisy chain structure

Fabrication of Interposer with 40μm TSVs

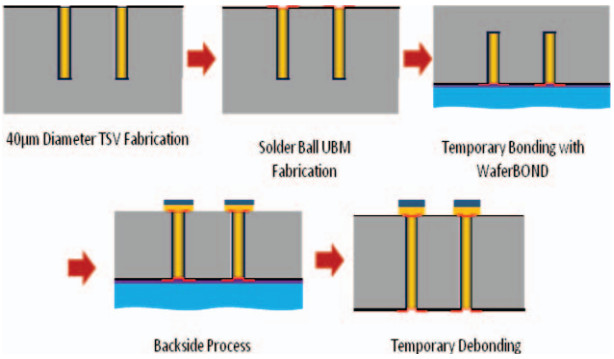


Fig.9 Process flow of Interposer with 40μm TSVs

Similar to the fabrication of test chip with 5μm TSVs, via holes of 40μm diameter, 180μm depth TSV interposer was formed by deep RIE and copper electroplating process, as shown in Fig.9. Fig.10 gives SEM image of 40μm TSV filling result. The current density of interposer electroplating was adopted as 1ASD, and the filling rate could achieve 100%.

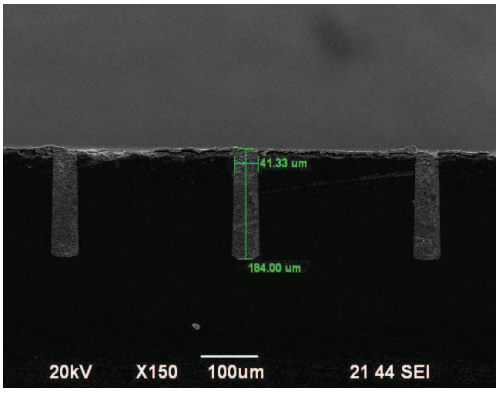


Fig.10 SEM image of 40μm TSV filling result

Final wafer thickness was thinned to 180μm. For interconnection between 5μm TSV chip and Si interposer, Cu/Sn bumps were plated after the deposition of TiW/Cu seed layer.

Assembly Process of 3D Integration Testing Vehicle

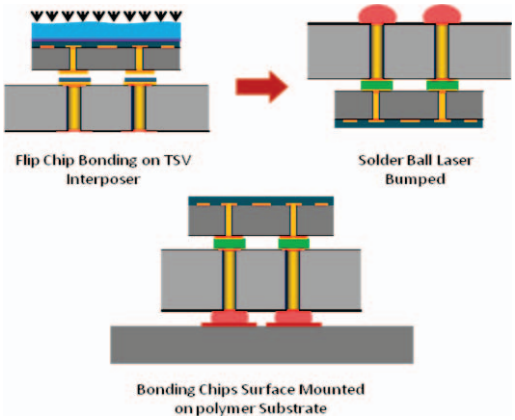


Fig.11 Assembly of 3D Stacking Structure

The assembly process of 3D stacking structure contains two parts shown in Fig.11. Firstly, test chip with 5um TSVs was stacked on TSV interposer by flip-chip bonding. Alignment marks were designed for flip-chip bonding using SUSS FC150 bonder with a higher alignment accuracy and no restricted camera area. Cu/Sn SLID (solid liquid inter-diffusion) bonding was adopted as the interconnect method in this bonding process[5].

In order to generate enough IMC (Intermetallic Compound) to form reliable metal eutectic bonding, the height of Cu microbump on test chip with 5μm TSVs was designed as 4μm, and the height of Cu/Sn microbump on interposer was 4μm Cu/3μm Sn. The bonding process profile is shown in Fig.12. The whole bonding process was under the protection of Formic acid and N_2 mixture.

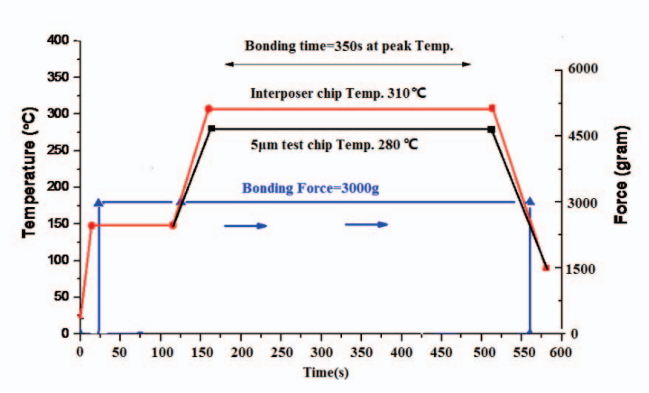


Fig.12 Bonding process of Cu-Sn-Cu

The stacking bonding structure of test chip with 5μm TSVs on TSV interposer was shown in Fig.13.

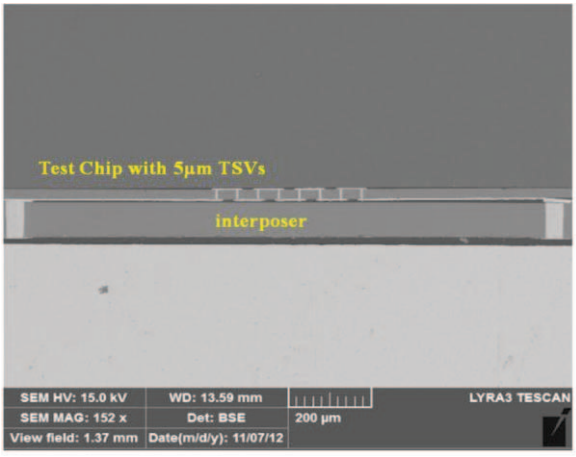


Fig.13 Stacking Bonding of test chip with 5μm TSVs on Interposer

The bonded chips were mounted on organic substrate. Fig.14 shows a finished testing vehicle through solder ball.

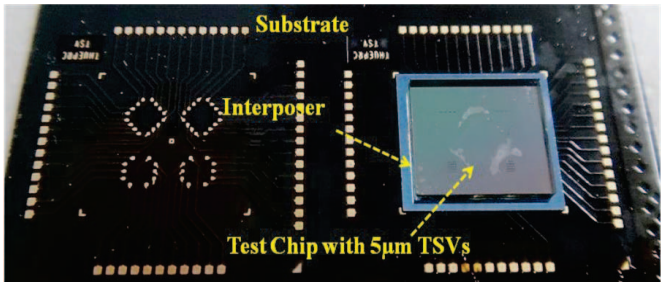


Fig.14 Testing vehicle of 3D stacking structure

Results and discussion

Fig.15 illustrates the X-ray images of the 3D stacking structure. The alignment accuracy of the assembly could be checked from the X-ray images, and the quality of the 3D assembly was also examined through X-ray.

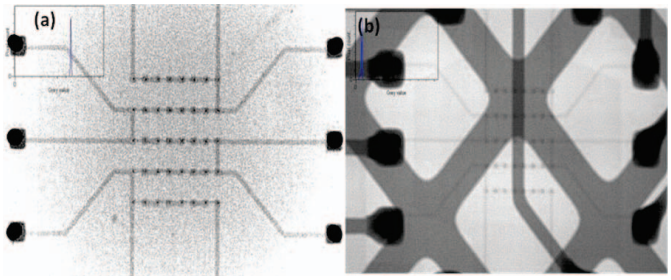


Fig.15 X-ray images of stacked structure (a)Flip chip bonding on TSV Interposer(b) Bonding chips mounted on BT substrate

Fig.16 presents the cross-section of 3D integration testing vehicle, which includes test chip with 5μm TSVs, interposer with 40μm TSVs and organic substrate.

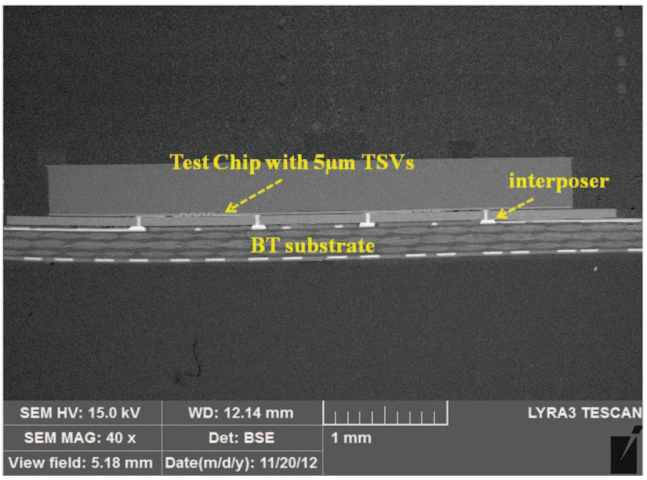


Fig.16 Cross-section of 3D integration testing vehicle

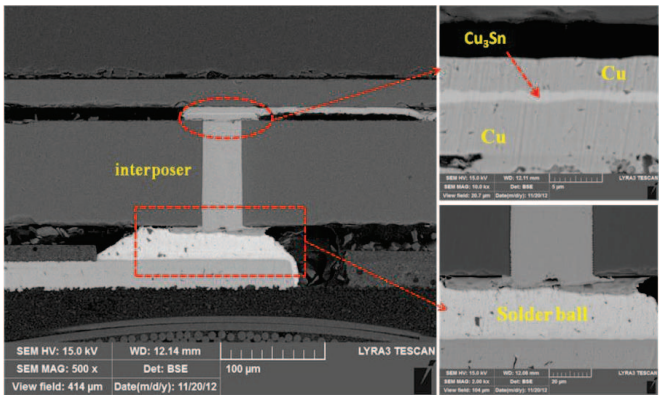


Fig.17 IMC between bonding interface

Fig.17 shows the IMC between bonding interface. Cu_3Sn was generated among the Cu-Sn-Cu bonding interface. The IMC layer between solder ball and Cu pad can be seen clearly from the SEM images.

Conclusions

In this paper, a testing vehicle with test chip and interposer was designed and fabricated. The test chip with 5μm TSVs was fabricated, and the key technologies in the fabrication process of 5μm TSV were introduced in detail. Robust copper electroplating process for 5μm TSVs with high aspect ratio up to 5:1 was realized by the high current density of 0.25ASD. Silicon wafer with 5μm TSVs was thinned to 25μm based on the good quality of temporary bonding.

The test chip with 5μm TSVs was assembled on the interposer with 40μm TSVs through Cu-Sn-Cu bonding, and the reliable metal eutectic bonding was formed. After that, the bonded module was assembled on designed testing board through solder ball laser bumped and reflow process.

Acknowledgments

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References

1. Tzu Kun Ku, "3D TSV Stacking IC Technologies, Challenges & Opportunities," *AMD Technical Forum 2011*
2. Ming-Jinn Tsai, "Overview of ITRI's TSV Technology, " *Trend Micro Titanium Internet Security 2011*
3. M. Jürgen Wolf, Thomas Dretschkow. *et al,* "High Aspect Ratio TSV Copper Filling with Different Seed Layers, " *2008 Electronic Components and Technology Conference*, 2008, pp. 563-569.
4. Ziyu Liu, Jian Cai, Qian Wang, Tao Wang, Tiwei Wei, Li Li, "Copper Chemical Mechanical Polishing and Wafer Thinning with Temporary Bonding for Through Silicon Via Interconnect, " *2012 International Conference on Electronic Packaging Technology & High Density Packaging,* 2012, pp. 488-493
5. SUH M-S, KWON H-S, "Growth Kinetics of Cu-Sn Intermetallic Compounds at Interface of 80Sn-20Pb Electrodeposits and Cu Based Leadframe Alloy, and Its Influence on the Fracture Resistance to 90.DEG.-Bending, " *Jpn J Appl Phys Part 1,* 2000, pp. 6067-6073.
6. J.U. Knickerbocker, P.S. Andry, B. Dang, R.R. Horton, C S. Patel. *et al,* "3D Silicon Integration, " *2008 Electronic Components and Technology Conference*, May. 2008, pp. 538- 543.
7. F. Inoue, T. Yokoyama, S. Tanaka, K. Yamamoto and S. Shingubara, "Addition of PEG-Thiol to Cu Electroless Plating Bath for Realizing Perfect Conformal Deposition in Through-Si Via Holes of 3-D Integration, " *ECS Transactions,* 25 (38) 2010, pp. 31-36.